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MONTEREY, CALIFORNIA

THESIS

DESIGN, ANALYSIS AND CONSTRUCTION OF A HIGH VOLTAGE CAPACITOR CHARGING SUPPLY

by

Nathan Tyler

June 2008

Thesis Advisor: Alexander L. Julian
Co-Advisor: William B. Maier II

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13. ABSTRACT (maximum 200 words)

The desire to use railguns in defense applications has elevated the level of concentration in all areas of the railgun system. Necessary in any railgun is a large amount of electric power to deliver the required force to the projectile. One popular source of power is high voltage capacitor banks. The NPS Railgun Lab employs a fully functioning railgun with capacitor banks as power supplies. A reliable and safe charging supply for these capacitor banks is desirable and investigated in this paper. Construction and testing of a power supply charger is compared to simulation results. The power supply charger consists of a Voltage Source Inverter (VSI) connected to a high voltage boost transformer; the output of the transformer is connected to a voltage doubler rectifier; the output of the rectifier charges the high voltage capacitor to 9 kV in two minutes. The power supply controller is an FPGA (Field Programmable Gate Array) with embedded control to ensure the safe operation of the power supply.

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DESIGN, ANALYSIS AND CONSTRUCTION OF A HIGH VOLTAGE CAPACITOR CHARGING SUPPLY

Nathan S. Tyler
Ensign, United States Navy
B.S., United States Naval Academy, 2007

Submitted in partial fulfillment of the
requirements for the degree of

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from the

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June 2008

Author: Nathan S. Tyler

Approved by: Alexander L. Julian
Thesis Advisor

William B. Maier
Co-Advisor

Jeffrey B. Knorr
Chairman, Department of Electrical and Computer Engineering

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ABSTRACT

The desire to use railguns in defense applications has elevated the level of concentration in all areas of the railgun system. Necessary in any railgun is a large amount of electric power to deliver the required force to the projectile. One popular source of power is high voltage capacitor banks. The NPS Railgun Lab employs a fully functioning railgun with capacitor banks as power supplies. A reliable and safe charging supply for these capacitor banks is desirable and investigated in this paper. Construction and testing of a power supply charger is compared to simulation results. The power supply charger consists of a Voltage Source Inverter (VSI) connected to a high voltage boost transformer; the output of the transformer is connected to a voltage doubler rectifier; the output of the rectifier charges the high voltage capacitor to 9 kV in two minutes. The power supply controller is an FPGA (Field Programmable Gate Array) with embedded control to ensure the safe operation of the power supply.

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LIST OF ABBREVIATIONS AND ACRONYMS

BNC – Bayonette Neil-Concelman connector

CT – Current Transformer

EMLF – electromagnetic Launch Facility

EMRG – Electromagnetic Railgun

FPGA – Field Programmable Gate Array

IGBT – Insulated Gate Bipolar Transistor

ISE – Integrated Software Environment

NEC – National Electric Code

NSWC – Naval Surface Warfare Facility

ONR – Office of Naval Research

PFN – Pulse Forming Network

PI – Proportional Integral

VHDL – VHSIC Hardware Description Language

VHSIC – Very High Speed Integrated Circuit

VSI – Voltage Source Inverter

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EXECUTIVE SUMMARY

The desire to use railguns in defense applications has elevated the level of concentration in all areas of the railgun system. The Naval Postgraduate School participates in research contributing to railgun defense applications. The Railgun laboratory at NPS maintains a firing railgun. This pulsed power weapon requires a large amount of energy to fire that is not readily available from typical AC or DC power sources. As a result, it becomes necessary to develop a means of delivering the required power in an effective manner. The power supplies for the rail gun are high voltage (~10kV) capacitors that are charged and subsequently discharged to deliver the necessary power to the railgun. Railgun power supplies are important to railgun use in defense applications. This research contributes to the ongoing investigation in usable railgun power supplies.

The first objective of this research was to develop a charger that charges the high voltage capacitors to a desired voltage. Additional objectives of this research were to determine the electrical and thermal stress on components selected for the charging supply and design a controller to ensure that peak current and voltage stresses are not exceeded.

The existing method of charging the capacitors in the railgun power supply involves an open-loop method of controlling the voltage on the capacitors. A 208 V AC source is manually controlled by a variac, boosted by a transformer, and then rectified by a diode bridge rectifier. The DC voltage at the output of the rectifier charges the capacitors in the power supply. The new solid state power supply charger achieves closed loop control of the voltage and current to the capacitors. By regulating the voltage on a capacitor, the charging rate is faster.

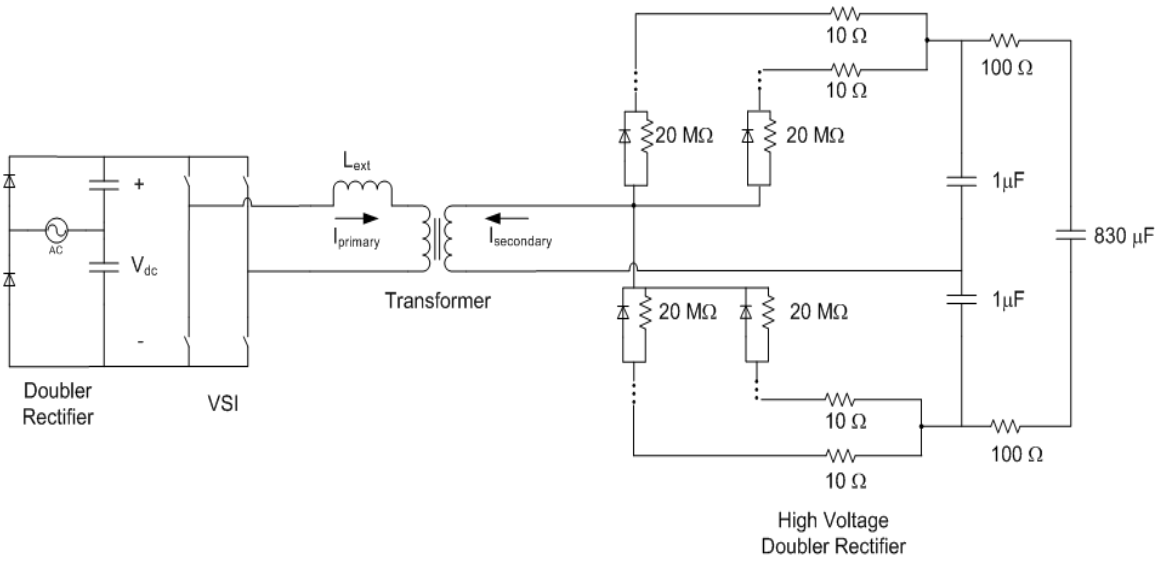

Figure 1. Simplified Circuit of charger (ellipses represent 6 additional diode/resistor pairs in series).

Figure 1 shows a simplified circuit diagram of the capacitor charger. This design contains three main components; a doubler rectifier and voltage source inverter (VSI), a transformer, and a high voltage doubler rectifier. The 208 V AC source is rectified and then inverted using an IGBT H-bridge to a controlled AC waveform. A transformer boosts the voltage and bucks the current. A high voltage doubler rectifier rectifies the high voltage waveform. The output of the high voltage doubler rectifier charges the high voltage capacitor.

The charger design was simulated to determine the behavior of the capacitor charger prior to selecting parts and construction. After parts selection and construction was completed, charger control was developed to meet the required objective of regulating capacitor charging. The charging of the capacitor is regulated by controlling the switching of IGBTs in the VSI. This control is performed by a field programmable gate array (FPGA), using two control loops: an inner current control loop and an outer voltage control.

Fault protection logic is incorporated to ensure safe functionality of the device. A voltage protection is included to prevent the charger from exceeding voltage thresholds. A current limiter is used to prevent damage to the secondary diode rectifier. A time

limiter is included to prevent the system from being on for longer than a desired time. Each of these protections shuts the converter off if a voltage, current, or time threshold is exceeded.

The completed charger was tested to a voltage of 8850 V. Each fault protection shut the charger off when a current, voltage, or time threshold was exceeded. The charger developed for charging the high voltage capacitors achieves the objective of charging the capacitor to a target voltage at an acceptable rate. Additionally, the fault protection logic protects the charger from current, voltage, and temperature failures with the current, voltage and time protections. Accurate simulation of the charger aided in the design, construction and control of the charger. Comparison of simulation and hardware waveforms is shown below.

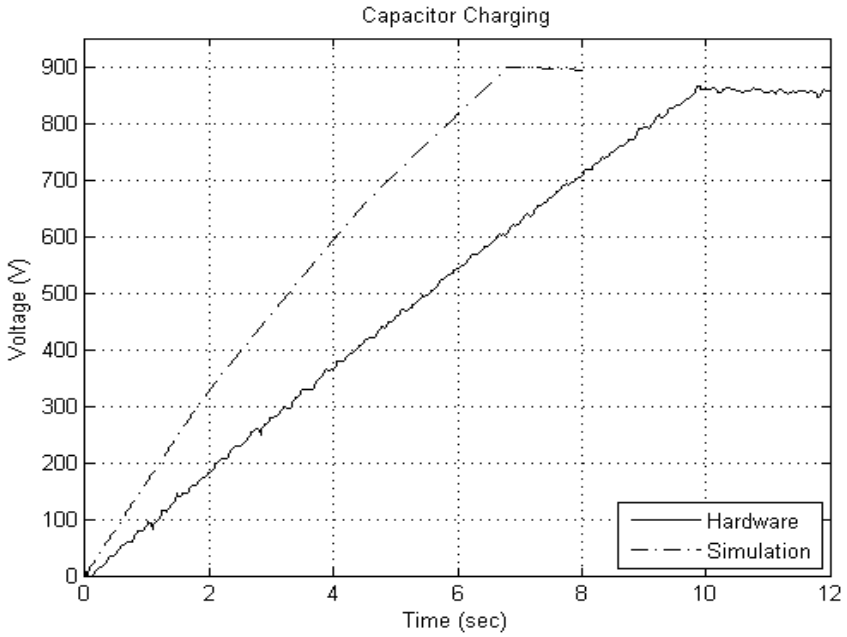

Figure 2. Capacitor Charging Comparison

Figure 2 compares charging capacitor voltage waveforms in simulation and the performance of hardware. Figures 3 and 4 compare hardware and simulation waveforms for the primary and secondary current of the charger respectively. These figures demonstrate the usefulness in using simulation in the design and construction of this high voltage capacitor charger.

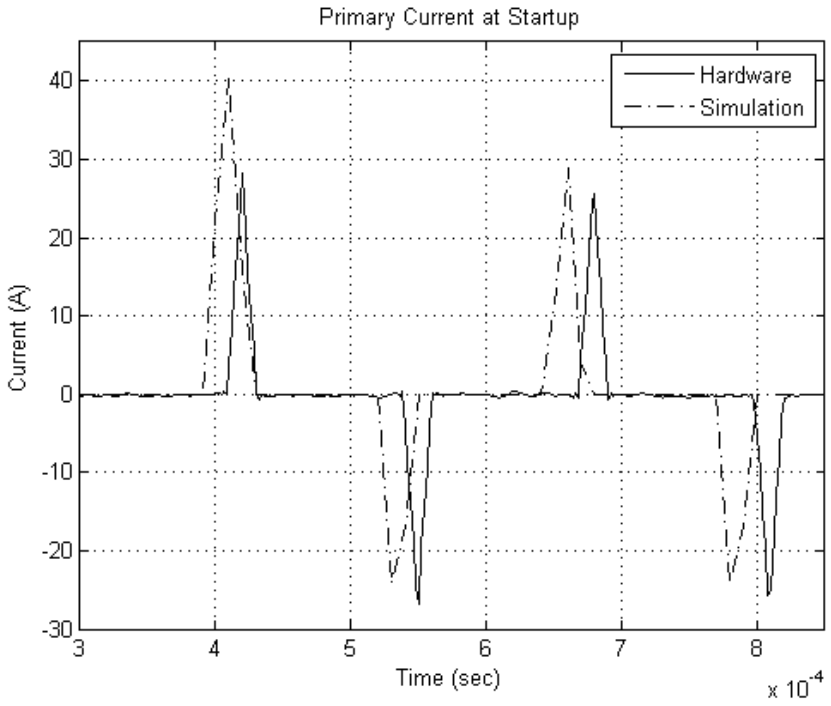

Figure 3. Primary Current Comparison at Startup

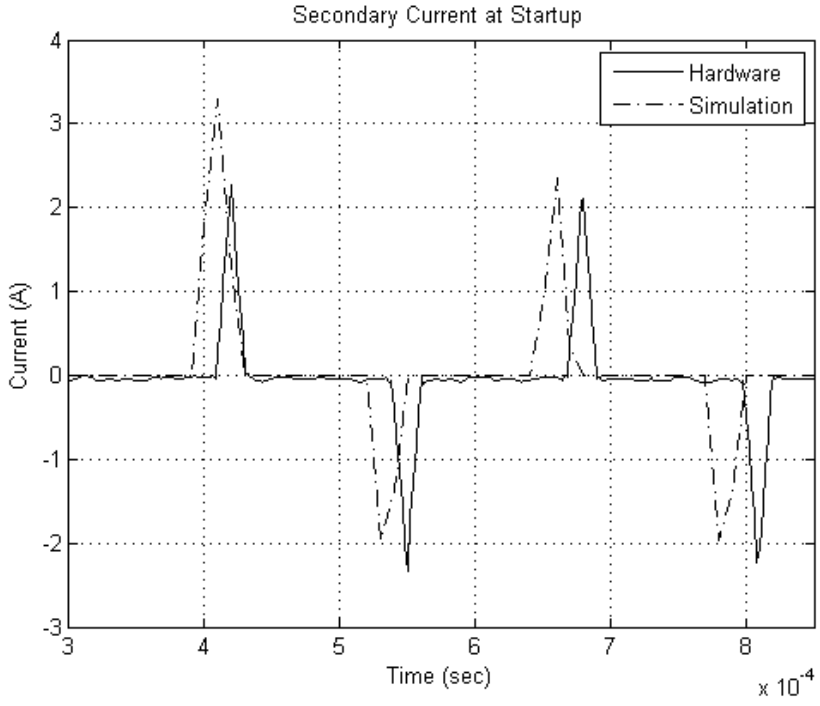

Figure 4. Secondary Current Comparison at Startup

Future research is important in the advancement of railgun technology. The development of effective power supplies for use in railgun defense applications is vital for future implementation.

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ACKNOWLEDGMENTS

I would like to thank Professor Alex Julian for guidance and teaching during this project. Thanks to Bill Maier for the opportunity to research railgun power supplies, as well as the use of the Railgun Laboratory and assistance throughout. Thanks to Gene Morris and Don Snyder for their all their help every time I asked. Finally, thanks to my family for being interested in what I'm doing.

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I. INTRODUCTION

A. PURPOSE

The Railgun Laboratory at the Naval Postgraduate School maintains a fully functioning railgun. This pulsed power weapon requires a large amount of energy that is not readily available from typical AC or DC power sources. Instead the energy comes from a pulse forming network (PFN) of high voltage (~10 kV) capacitors that are charged and subsequently discharged to deliver the necessary power to the railgun.

The existing method of charging the capacitors in the power supply involves an open-loop method of controlling the voltage on the capacitors. A 208V AC source is manually controlled by a variac, boosted by a transformer, and then rectified by a diode bridge rectifier. The DC voltage at the output of the rectifier charges the capacitors in the power supply. This method is effective and simple but is limited in two primary areas. First, a human component is needed to control the voltage across the capacitors, which is somewhat dangerous in the case of a misfire of the capacitors, as the individual observing the charging of the power supplies is close to the supplies. Second, with open loop control, the desired set point voltage is not controlled and can cause errors in energy input to the railgun.

The new power supply achieves closed loop control of the voltage and current to the capacitors. By regulating the voltage on a capacitor, the charging rate is faster. At the same time this controller reduces the voltage droop of the capacitors after reaching desired voltage. With automated charging of the capacitor, the human control component needed in the open-loop method is removed and the charging of the capacitors becomes safer for the technicians. Additionally, the automation provides safety features such as limitations on the current to the capacitors and prevents over charging the capacitors. This thesis describes the design, construction and employment of a power converter to charge a capacitor.

B. RAILGUN OVERVIEW

The mission of the Electromagnetic Railgun (EMRG) Innovative Naval Program is "to develop the science and technology necessary to design, test, and install a[n]…EMRG aboard United States Navy Ships in the 2020-2025 timeframe [1]." As of March 2008, the Office of Naval Research (ONR) is testing a functioning 32–mega joule railgun at the Electromagnetic Launch Facility (EMLF) at the Naval Surface Warfare Center (NSWC) in Dahlgren, VA.

Railguns have long been considered as potentially significant military weapons because they accelerate projectiles to high speeds (~2.5 km/s) [2]. These weapons have applications in the U.S. Navy to provide long range Naval surface fire support and in the U.S. Army in armor penetration. An added benefit is the elimination of chemical propellants as a firing mechanism.

The power requirements of firing such a weapon are massive. The gun itself is driven by supplying a large amount of current to two rails (hence *rail*gun) and using the resultant magnetic field to propel a projectile. In the NPS Railgun Laboratory and the EMLF this current is supplied by the using a PFN created by discharging high voltage capacitors. The primary focus of this thesis is the development of power electronics to safely and efficiently control the charging of the NPS high voltage capacitors.

C. APPROACH

A safe and effective method of charging the high voltage capacitors is needed. A topology of a boost converter is used in order to *boost* the voltage. Simulation of this topology determines transient and steady state behavior of the charger. The construction of the charger is based on the design simulated. Charger control uses a Xilinx FPGA (Field Programmable Gate Array) to control an H-bridge of IGBTs (Insulated Gate Bipolar Transistors). The Xilinx blockset operating in the Simulink environment develops the control algorithms for the charger. The waveforms generated by the charger were compared to the simulation waveforms to validate the design process.

The thesis is organized as follows. Chapter II contains a background of design issues. Chapter III contains an overview of the charger topology and describes the main components of the charger. Chapter IV discusses the charger hardware and Chapter V addresses the control organization. Chapter VI shows the waveforms during charger operation and compares important simulation waveforms to the performance of the hardware, and Chapter VII describes the conclusions and possibilities for further research.

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II. BACKGROUND

A. CAPACITOR CHARGING

The capacitors used to fire the railgun are General Atomics Series C High Voltage Energy Storage Capacitors, are rated at 11 kV and have a capacitance of 830 μF with 50 kJ stored energy. This energy is then rapidly discharged (on the order of milliseconds) to fire the railgun.

The existing method of charging the capacitors in the NPS Railgun Laboratory includes boosting 208 V_{rms} AC with a voltage boosting transformer and then rectifying the boosted voltage. The circuit diagram for this method of charging these capacitors is shown in Figure 5.

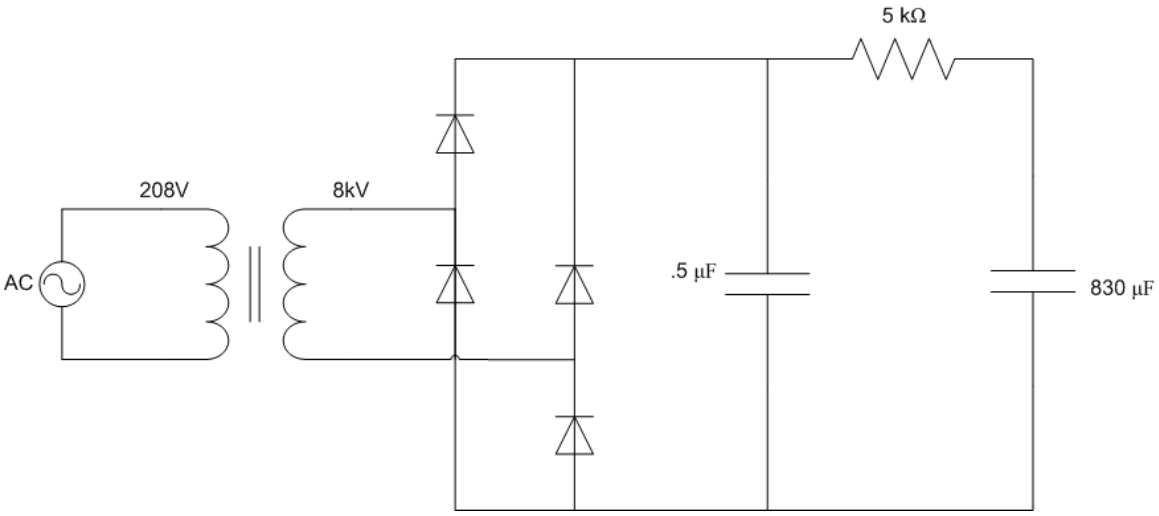

Figure 5. Circuit Diagram of Existing Capacitor Charger.

The AC wall source supplies 208 V_{rms} to a step-up transformer that boosts the voltage to approximately 9 kV. A full bridge rectifier then rectifies the AC waveform. The parallel-series set up of the 0.5 μF capacitor and 5 kΩ resistor simultaneously provide a filtering effect and limit the current to the charging capacitor (the 830 μF load). This method of charging the capacitor is open loop control, where a lab technician observes the voltage on the power supply and adjusts the input voltage according to the error. This technique of charging the capacitor works but has limited controllability and

involves a human component. In addition, there is little control to the charging of the capacitors other than current limiting resistors.

Different methods of charging high voltage capacitors exist. Solid-state switching is a common means of supplying the desired energy to capacitors. A voltage boosting transformer can be used to boost the output of a Voltage Source Inverter (VSI) and the output of the transformer can be rectified [3],[4],[5]. With solid state devices the charging of the capacitor can be controlled digitally and control input changes can be made quickly and accurately.

B. HIGH VOLTAGE CONCERNS

The National Electric Code (NEC) in the United States defines *high voltage* as any voltage over 600 V [6]. According to this definition the voltages (1 – 10 kV) at which these capacitors are charged exceeds the NEC benchmark. Concerns at these voltages include the need to contain such potentials within safe parameters. When building equipment designed to sustain high voltages two parameters must be taken into consideration: creepage and clearance. "Creepage distance is the shortest distance between energized parts…along the surface of an insulating material. Clearance is defined as "the shortest point to point distance in air between uninsulated energized parts [7]." Creepage and clearance become critical factors because their oversight can lead to equipment failure.

To eliminate high voltage issues, proper care is taken in the construction of the elements of the power charger which sustain such voltages. The distance between charger components that would be exposed to these voltages is kept at distances of at least two inches. Any connection to ground near the high voltage components is covered with high voltage protective tape. The metal casing of the charger is bonded to ground. The transformer, which sustains voltages that exceed the NEC benchmark, is wrapped in protective high voltage tape, and care was taken to ensure the tape's continuity. Further discussion of transformer design and construction will be discussed later.

C. CHARGER CONTROL – THE FPGA

An effective and readily available means of controlling the solid state switches is a Xilinx Field Programmable Gate Array (FPGA). FPGAs are semiconductor devices that contain programmable logic elements (such as AND and OR gates, or more complex logic) that can be programmed to perform certain functions. In this case, the function is used to control the switching of the solid state IGBTs in the VSI. In addition to controlling the VSI, the firing of the capacitor is controlled through logic programmed into the same FPGA.

A Xilinx Virtex-II XC2V1000 is the FPGA used for this application. The FPGA is programmed by using the Xilinx Blockset in the Simulink environment. This software provides a user-friendly means of programming the FPGA in an effective and repeatable manner without having to know VHDL (VHSIC (Very-High-Speed Integrated Circuits) Hardware Description Language). By creating the software with the Xilinx Blockset in Simulink, the user can then generate VHDL code using the Xilinx System Generator, a block in the Xilinx Blockset. After VHDL generation, the user compiles the VHDL code using Xilinx ISE (Integrated Software Environment). After the code is compiled it is then ready to be loaded on the FPGA. This high-level design provides a means for the engineer to design a wide variety of tools for use in a wide array of applications. Though it is not necessary to know VHDL, it is quite beneficial for the user to be comfortable with discrete processing techniques, fixed point math, and combinatorial logic in digital control applications.

A control board is integrated to the FPGA board. This board enables the pins of the FPGA to be easily accessed through BNC (Bayonette Neil-Concelman) connectors. There is also a 4-channel, 12-bit A/D converter to provide measurement capabilities to the FPGA. Because the FPGA may not supply adequate voltage to the device being driven (such as gate drivers or logic circuits), level shifters are also included.

Integrated together this package provides control solutions for a wide variety of applications. In addition to the fact that these tools were readily available, this FPGA is particularly suited to this application for a number of reasons. First, the FPGA and

control board integrates easily with the VSI: the only connections to be made were the BNC cables. Measurements are easily taken with an A/D converter. Turning the charger on/off and firing the capacitors is simplified through a fire and control system that was programmed into the FPGA, which will be discussed later in this thesis.

Perhaps the greatest benefit to using this FPGA configuration is through the use of Chipscope, an integrated signal analyzer accessible through software on a PC. Chipscope is able to program, interact with, and retrieve data from the FPGA, making it extremely useful throughout the design and construction of the charger.

III. CHARGER TOPOLOGY

A. TOPOLOGY OVERVIEW

The topology of the capacitor charger is discussed in the following section. Figure 6 shows a simplified circuit diagram of the charger.

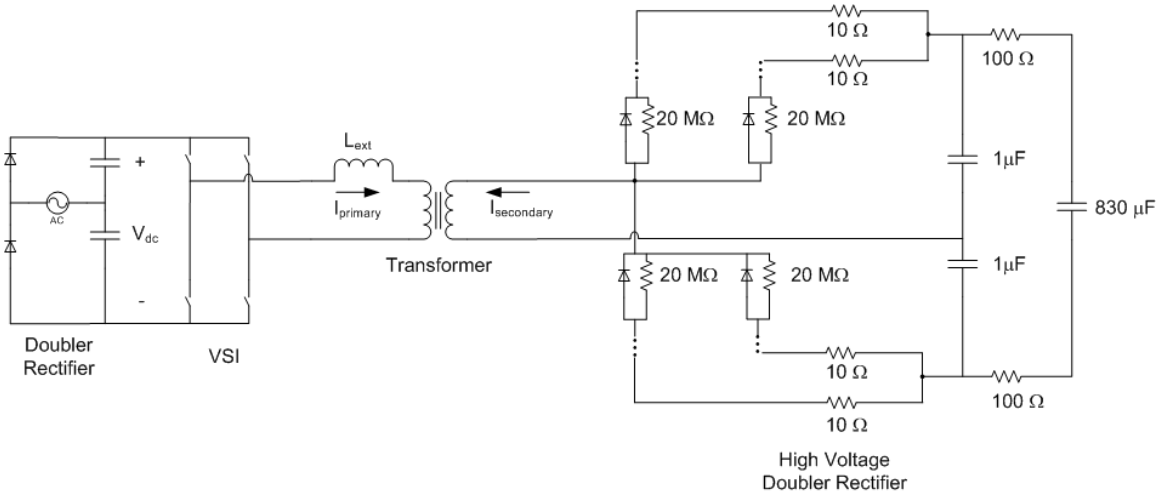

Figure 6. Simplified Circuit of charger (ellipses represent six additional diode/resistor pairs in series).

The AC Power source in the left of the figure signifies the 208 V_{rms} source, which is rectified and doubled in the first doubler rectifier and becomes the DC bus voltage (labeled V_{dc}) as shown. The set of four switches signify the VSI, H-bridge which goes to the boosting transformer. The secondary set of windings of the transformer is wired to the high voltage doubler rectifier. The output of the rectifier is connected to the positive and negative terminals of the high voltage capacitor. The VSI, the transformer, and the rectifier will be discussed in detail.

1. Doubler Rectifier and Voltage Source Inverter (VSI)

The doubler rectifier works as follows. Each capacitor is charged to approximately the peak of the AC input voltage. The top capacitor in the DC bus is charged through the top diode during the positive cycle; the bottom capacitor is charged through the bottom diode during the negative half cycle. The resulting DC bus voltage is

the sum of the peak AC input voltage [8]. With a 208 V_{rms} source (295 V peak), the doubler rectifier has an output of 595 V DC. The DC voltage is then inverted to a controlled waveform in the VSI. The VSI consists of an H-bridge of IGBTs which create a single phase AC waveform. The switching of these IGBTs is controlled by the FPGA which reads in high voltage capacitor voltage and the primary current and makes control decisions, varying the IGBT duty cycle depending on the charging of the capacitors.

2. Transformer

The output of the VSI goes to the boosting transformer. This transformer consists of primary and secondary windings with the direction of the positive current shown above. An external leakage inductance (labeled L_{ext} in Figure 6) is added to limit the *di/dt* of the primary current. The external leakage inductance is lumped together with the leakage inductance of the transformer. A description of an idealized transformer model follows.

A transformer is a magnetically coupled circuit used for the purpose of changing the voltage and current levels in a circuit. As this design utilizes a two winding transformer, this discussion will be limited to a transformer with two windings. The voltage equations for a two winding transformer may be expressed as [10]

$$\begin{aligned} v_1 &= r_1 i_1 + \frac{d\lambda_1}{dt} \\ v_2 &= r_2 i_2 + \frac{d\lambda_2}{dt} \end{aligned} \qquad (1)$$

where the subscripts 1 and 2 refer to the primary and secondary windings respectively. The term r refers to the resistance in the coil; i refers to the current in each coil, and λ refers to the flux linkages related to coils 1 and 2. These equations may be written in matrix form as [10]

$$\mathbf{v} = \mathbf{ri} + \frac{d\lambda}{dt} \qquad (2)$$

where

$$\mathbf{r} = \begin{bmatrix} r_1 & 0 \\ 0 & r_2 \end{bmatrix} \quad (3)$$

and

$$\lambda = \begin{bmatrix} \lambda_1 \\ \lambda_2 \end{bmatrix} \quad (4)$$

This design utilized such a large magnetic core for the transformer such that saturation would not be a problem. Neglecting saturation, the system becomes linear and the flux linkages may be described as follows [10]

$$\lambda = \mathbf{L}\mathbf{i} \quad (5)$$

where the inductance matrix **L** is broken down as follows [10]

$$\mathbf{L} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} = \begin{bmatrix} L_{l1} + L_{m1} & L_{m1} \\ L_{m2} & L_{l2} + L_{m2} \end{bmatrix} \quad (6)$$

The leakage inductances are L_{l1} and L_{l2} and the magnetizing inductances of coils 1 and 2 are L_{m1} and L_{m2}, respectively. The external leakage inductance is lumped with the leakage inductance of the primary windings. L_{11} and L_{22} are the self inductances of coils 1 and 2, and the mutual inductances are defined as L_{12} and L_{21} [10]. Ideally, L_{12} and L_{21} are equal.

Using the equation (5), the voltage equations in matrix form become

$$\mathbf{v} = \mathbf{r}\mathbf{i} + \mathbf{L}\frac{d\mathbf{i}}{dt} \quad (7)$$

With this equation it becomes possible to simulate the voltages and currents of the transformer, solving for the primary and secondary currents. This method was used in the Simulink model subsystem "Magnetics." Using the current as a state variable, the equation becomes

$$\frac{d\mathbf{i}}{dt} = \mathbf{L}^{-1}(\mathbf{v} - \mathbf{r}\mathbf{i}) \Rightarrow \mathbf{i} = \int \mathbf{L}^{-1}(\mathbf{v} - \mathbf{r}\mathbf{i})dt \quad (8)$$

The output voltage of the charger can be calculated:

$$V_{HV} \leq 2V_{DC}\frac{N_2}{N_1} \qquad (9)$$

where V_{HV} is the high voltage output of the rectifier, V_{DC} is the voltage on the DC bus, and $\frac{N_2}{N_1}$ is the turns ratio for the transformer. Multiplying by 2 is a simple calculation to account for the voltage doubler at the output of the rectifier. The DC bus voltage with the rectified 208 V_{rms} AC input is 595 V_{dc}. Using this value the turns ratio $\frac{N_2}{N_1}$ can be adjusted to achieve the desired output voltage V_{HV}. This yields a turns ratio of 10:1 to boost to a theoretical voltage of 12,000 V. Limitations of the components of the system, such as the lifetime of the high voltage capacitors preclude the operator from reaching such voltages.

3. High Voltage Doubler Rectifier

The output of the transformer feeds the high voltage doubler rectifier, as seen in Figure 6. This doubler rectifier works exactly the same as the doubler rectifier supplying the DC bus voltage, only at much higher voltages and at a different frequency. The ellipses in the figure signify a diode/resistor string of 6 additional diodes in series for a total of 7 diode/resistor pairs on each part of the bridge. The 20 MΩ resistors are in parallel to protect the diode. The 1 μF capacitor banks are actually 10, 0.1 μF capacitors in parallel. These two banks act as a voltage doubler and boost the voltage to the output capacitor, the 830 μF capacitor. The 10 Ω resistors divide the current evenly between each diode string. The two 100 Ω resistors in series with the 830 μF capacitor dissipate energy upon capacitor discharge. The high voltage capacitor has a reverse voltage after discharge, and these two resistors dissipate this reverse voltage energy.

B. SIMULATION

Matlab's Simulink simulation environment was used to predict the behavior of the charger before actual construction. Figure 7 shows the topmost level of the simulation for the railgun charging supply.

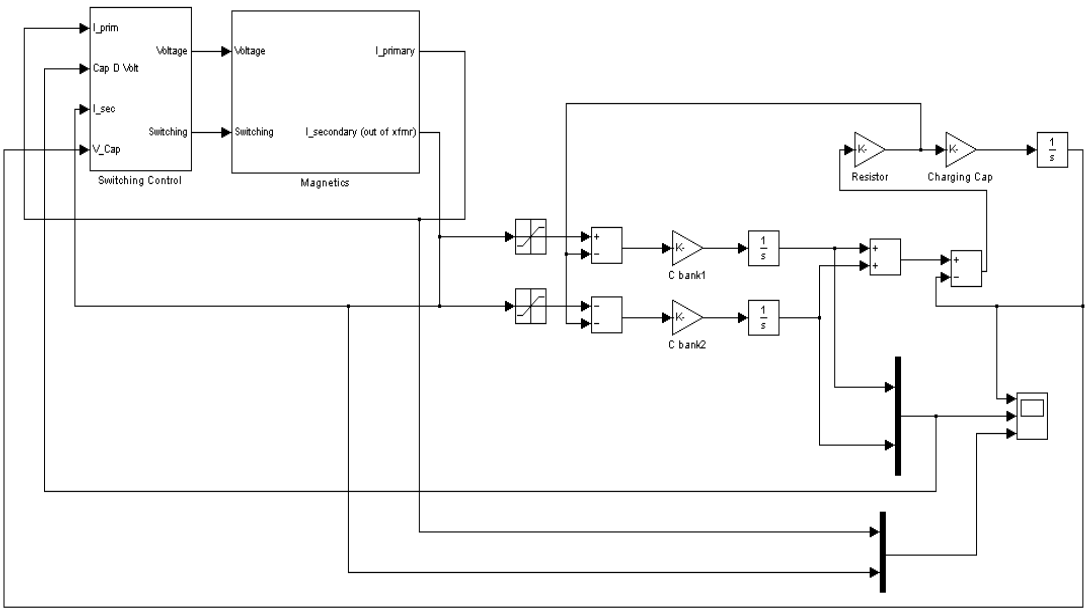

Figure 7. Top Level of Simulation [9] (Standard Simulink symbols are used).

This simulation includes all elements mentioned in section III.A; the VSI, the transformer and the high voltage doubler rectifier. The subsystem "Switching Control" contains the algorithmic elements included in the FPGA to control the VSI, as well as the logic for the switching elements of the VSI. The subsystem "Magnetics" includes the calculations for the transformer magnetics based on the inductance values measured experimentally. The external leakage inductance is included as a parameter of the transformer. The output of the transformer (reading "I_secondary (out of xfmr)") is the secondary current. This current is sent through the simulated rectifier (the saturation blocks) then through the capacitors (the gains "C-bank" and integrators). The resultant voltages are summed and sent through the output resistors (gain block "resistor"), which becomes the current sent into the charging capacitor. The charging capacitor is then simulated by the "Charging Cap" gain and the integrator.

Figure 8 shows the subsystem "Magnetics." The equations describing the computation of the voltages and currents in this subsystem are described in section III.A.2.

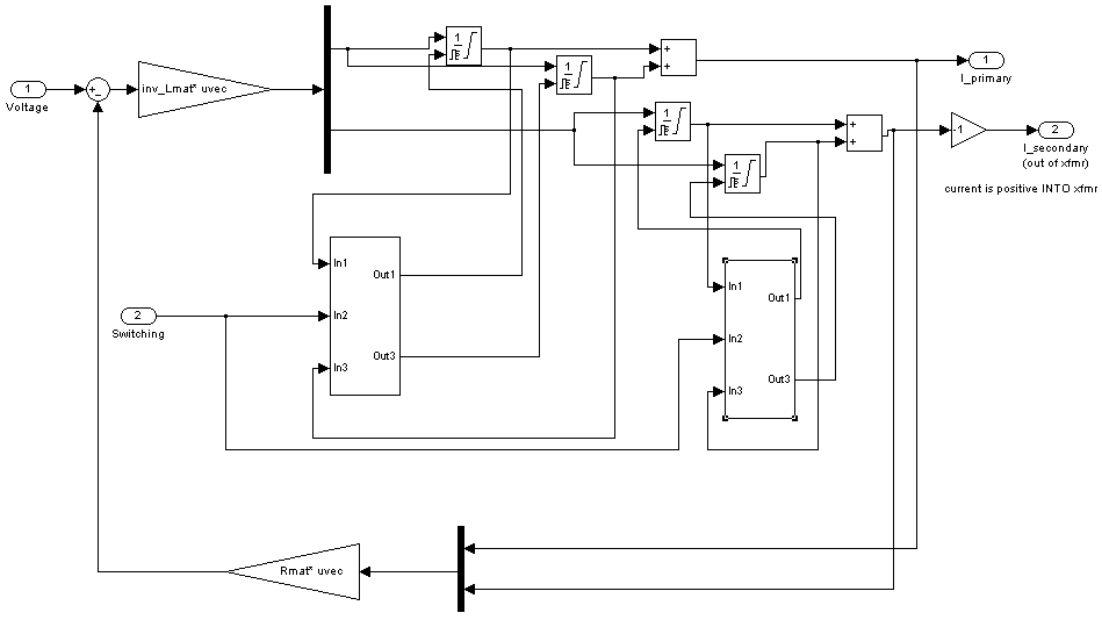

Figure 8. Inside Subsystem "Magnetics" [9] (Standard Simulink symbols are used).

Figure 9 shows the subsystem "Switching Control." A 4 kHz sawtooth wave is generated by integrating the constant "fmod." This sawtooth wave is compared to a duty cycle generated in the subsystem "Control." When the duty cycle is greater than the sawtooth, the IGBTs are switched on. To prevent the IGBTs from turning on more than once per switching period, control logic was also added. The whole of this control logic is computed in the subsystems "A+ B- Switch Control" for one half of the H-bridge and "A- B+ Switch Control" for the other half.

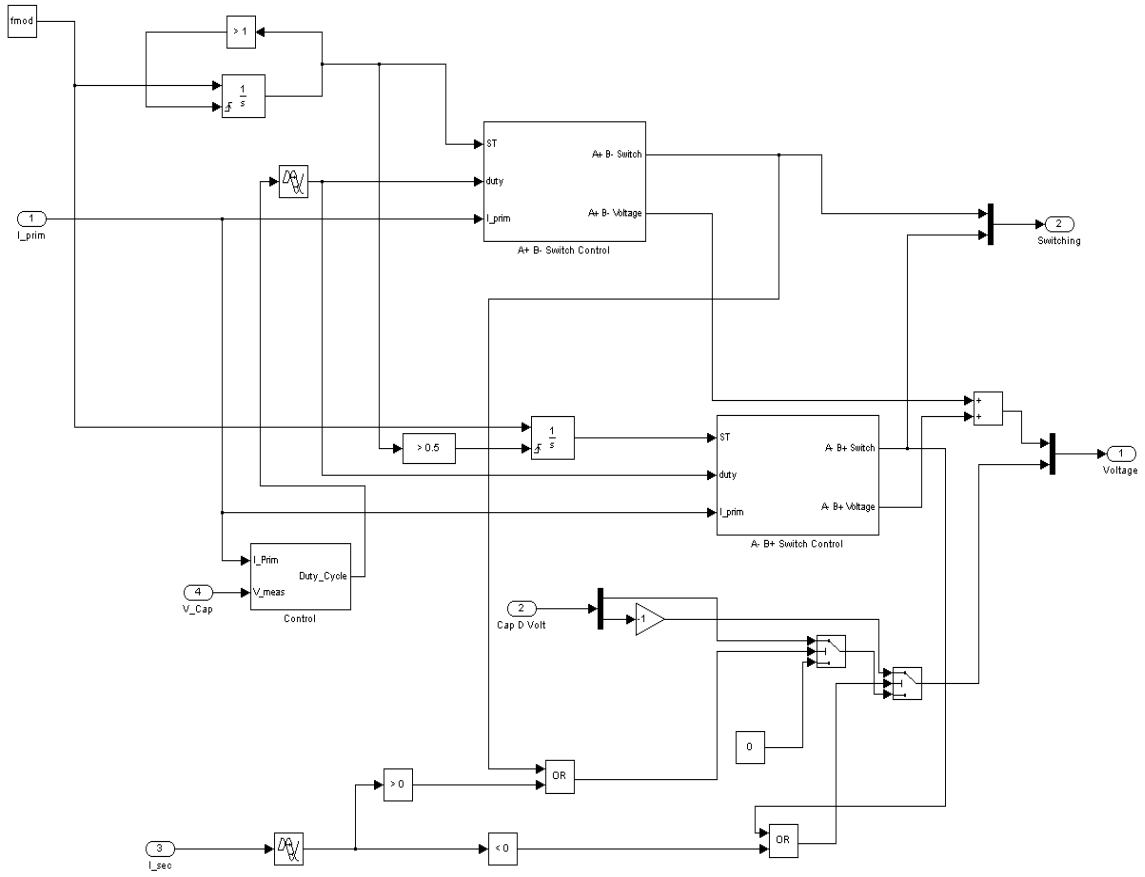

Figure 9. Inside Subsystem "Switching Control" [9] (Standard Simulink symbols are used).

The subsystem "Control" reads in the value of the high voltage capacitor and uses the error between desired capacitor voltage and actual to compute a current reference using a PI controller. A feed-forward term is added to this current reference to improve the rate of charging the high voltage capacitor. This current reference is compared to the measured current and sent through an additional PI controller to compute a duty cycle. This duty cycle is compared to the sawtooth waveform to switch the IGBTs on.

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IV. CHARGER HARDWARE

A. DOUBLER RECTIFIER AND VSI

The doubler rectifier and VSI used for this application is a combined package SEMIKRON SEMISTACK three phase rectifier and inverter. The SEMISTAK was modified slightly to enable the operation of a doubler rectifier. Only one phase of the rectifier and inverter is used. The 208 V AC source was rectified using a full wave rectifier in the SEMISTACK module. A DC bus voltage is maintained constant in a capacitor bank acting as a voltage multiplier. The multiplier maintains the DC bus voltage at approximately 595 V when the inverter is off.

The rectifier used in the SEMISTACK is a SEMIKRON SKD 51/14 three phase rectifier. The capacitor bank is made up of two 2200 μF capacitors. A lead is connected between the two capacitors in series to create the voltage multiplier. These capacitors are sensitive to inrush current. To limit this inrush current applied to the capacitors during operation of the charger, two thermistors are placed at each lead of the AC source into the rectifier and capacitors.

The IGBTs are SKM 50 GB 123D IGBTs. These IGBTs are driven by SEMIKRON SKHI 22 gate drivers. The gate drivers are controlled by the output of the FPGA. As mentioned previously, only a single phase of the three phase inverter is utilized, creating an H-bridge configuration for the inverter. The datasheet for the SEMIKRON SEMISTACK is included in the Appendix.

B. TRANSFORMER

According to simulation, the desired voltage boost ratio at the outset of design is ten to one. This ratio changed as design proceeded and difficulties in dealing with the magnetics persisted. The transformer was built in house with a Metglas AMC 630 C-core. Initially the transformer was wound with the primary on one side and the secondary on the other. However, because of the dimensions of the core, this configuration does not

provide enough flux linkage to give the adequate boost in voltage. The windings are instead placed with the secondary on top of the primary, which improves the flux linkage yielding better results. The final turns ratio used is 158:13 yielding approximate boost ratio of 12 to 1.

To limit the change in current over a period of time at the output of the inverter, a leakage inductance is placed in series with the output of the VSI, as shown in Figure 6. The core for this inductor is an Arnold MP-2205205-2 powdered core. The datasheets for the Metglas AMC 630 C-core and the Arnold MP-2205205-2 are available in the Appendix.

Final winding of the transformer allows measurement of the device's parameters to produce accurate simulation of the hardware. These parameters are measured with the transformer not installed in the charger. With a series of open and short-circuited measurements the values of the matrices in equations (3) and (6) are determined. In (3), the resistance r_1 represents copper losses in the primary windings and r_2 represents copper losses in the secondary. In (6), L_{l1} represents the leakage inductance of the primary windings. The mutual inductance between winding one and winding two is represented by L_{m1}. The mutual inductance between winding two and winding one is L_{m2},. The leakage inductance of winding two is L_{l2}. It is assumed that core losses are lumped into the winding losses.

Using the equations in (10) for referencing inductances and assuming that 96% of leakage inductance is on the primary windings [10], the inductance values of the transformer are determined. The primary and secondary resistances are measured directly with an ohmmeter. The inductance values are measured with an impedance meter with open and short-circuit configurations. Primed variables indicate values referred to the opposite winding. Measuring on the primary and an open circuit on the secondary yields $L_{l1} + L_{m1}$. A short circuit on the secondary measuring on the primary gives $L_{l1} + L_{l2}^{'}$. An open circuit on the primary and measuring on the secondary gives $L_{l2} + L_{m2}$. A short circuit on the primary and measurement on the secondary

yields $L_{l1}^{'} + L_{l2}$. Measurements and inductance values are shown in Table 1. All inductance values are in milli-Henries, resistances in ohms.

$$L_{l2}^{'} = \left(\frac{N_1}{N_2}\right)^2 L_{l2}$$
$$L_{l1}^{'} = \left(\frac{N_2}{N_1}\right)^2 L_{l1} \qquad (10)$$
$$L_{l1} = 0.96(L_{l1} + L_{l2}^{'})$$

Measured Values		Extrapolated Values	
$L_{l1} + L_{m1}$	1.89 mH	L_{m1}	1.88 mH
$L_{l1} + L_{l2}^{'}$	0.0134 mH	L_{m2}	266 mH
$L_{l2} + L_{m2}$	267 mH	L_{12}	22.89 mH
$L_{l1}^{'} + L_{l2}$	2.33 mH	L_{21}	21.86 mH
r_1	0.05 Ω	L_{l1}	0.0067 mH
r_2	2.56 Ω	L_{l2}	1.34 mH

Table 1. Measured Transformer Parameters

These are the values of the transformer model. The turns ratio on the final transformer is 158 secondary to 13 primary, giving a boost ratio of 12.15.

C. HIGH VOLTAGE DOUBLER RECTIFIER

The diodes used in the rectifier are Vishay RGP02-20E ultrafast rectifier diodes. These diodes have a maximum repetitive peak reverse voltage of 2000V and have a maximum peak forward surge current of 20 A. Placing these diodes in series increases the reverse blocking capabilities up to 14,000 V for a string of 7 diodes. In order to protect the diode string from reaching avalanche breakdown, a high value resistor (20

MΩ) is placed in parallel with each diode. These resistors divide the rectifier output voltage across each diode to prevent any one diode from reaching the avalanche breakdown voltage.

The capacitors used for the voltage doubling capacitor bank are ASC 6000V DC 0.1 μF capacitors. This rectifier doubles the output voltage; the 20 MΩ resistors divide the voltage evenly on the rectifier. The 1 μF capacitor banks create a more constant output voltage. The 10 Ω and 100 Ω resistors used are Ohmite resistors, AW100KE and AY101KE respectively. The datasheet for the ASC capacitors and the specifications for the Ohmite resistors can be seen in the Appendix.

V. CONTROL DESIGN

A. CONTROLLING CAPACITOR CHARGING

The charging of the capacitor is regulated by controlling the switching of the IGBTs. This control is performed by an FPGA which uses two control loops: an inner current control loop and an outer voltage control. An added benefit of controlling the capacitor charging is that the FPGA is used to prevent devices in the converter from being damaged. Discussion now turns to the hardware and software of the voltage and current control loops, beginning with the voltage control.

1. Voltage Control

The output voltage of the converter is reduced by a voltage divider by 100. The output of the voltage divider is measured by a Tektronix P2500 High Voltage Differential Probe. Because this probe requires high impedance at termination which is not present at the A/D Converter input, a unity gain inverting operational amplifier is used provide adequate termination impedance for the probe. The output of the op amp is then connected to the A/D converter. The op amp circuit is shown in Figure 10. With a reduction by 100 in the voltage divider and an attenuation of approximately 52 in the probe, the amplification required to give accurate voltage is -5200.

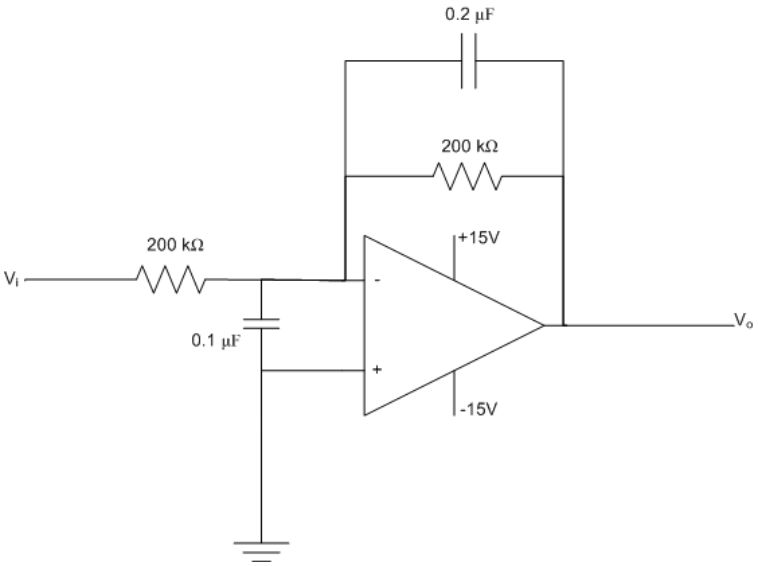

Figure 10. Operational Amplifier Circuit

The desired charge voltage is sent from the firing and control board to the FPGA. More will be discussed concerning the firing and control board at a later point. This desired voltage (the "V_Des" signal) is compared to the actual voltage measured by the high voltage probe (the "V_meas" signal). The error signal is then sent through a PI controller, the output of this PI controller is the reference signal for the current controller (the "I_ref" signal). The voltage control algorithm in Simulink/Xilinx environment is shown in Figure 11.

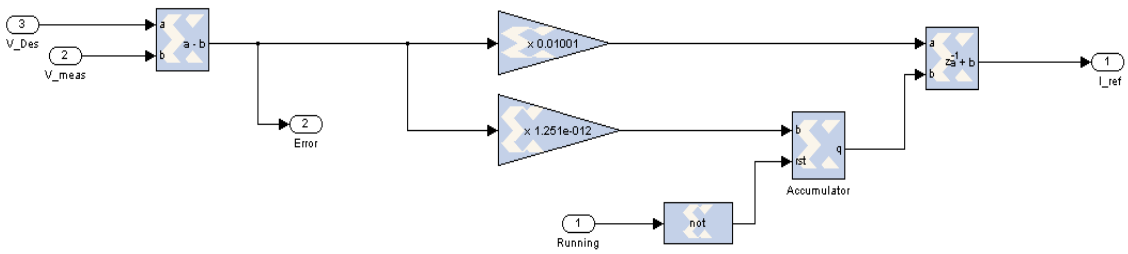

Figure 11. Voltage PI Control Block Diagram

The accumulator is driven by the "Running" signal, a signal that keeps the converter on as long as there is no fault. The error signal is sent out to feed-forward control, discussed in the next section.

2. Current Control

The output of the voltage PI controller is a current reference added to a feed-forward term with logic as follows. When the converter is turned on, a feed-forward value is added to the current reference signal to accelerate the charging of the capacitor. When the converter reaches charge voltage, determined by comparing voltage error to zero, the feed-forward term is removed, and the current reference is reduced to a smaller value to compensate the losses due to leakage current in the thyristors at high voltage. The current PI controller is the same logic as the Voltage PI controller. The current sensor is an LT 100-S SP30 current transformer (CT). The gain on this CT was also verified by comparing Chipscope measurements and oscilloscope measurements, as with the voltage probe. The datasheet for the LT 100-S SP30 can be seen in the Appendix.

Figure 12 shows the overall voltage and current regulation computational algorithm with feed-forward logic. The output of the current PI controller is the duty cycle that drives the on/off signal of the IGBTs. While voltage regulation alone would be effective in achieving the desired charge voltage of the capacitors, regulating the current protects the diodes in the high voltage rectifier from exceeding their average current limitations.

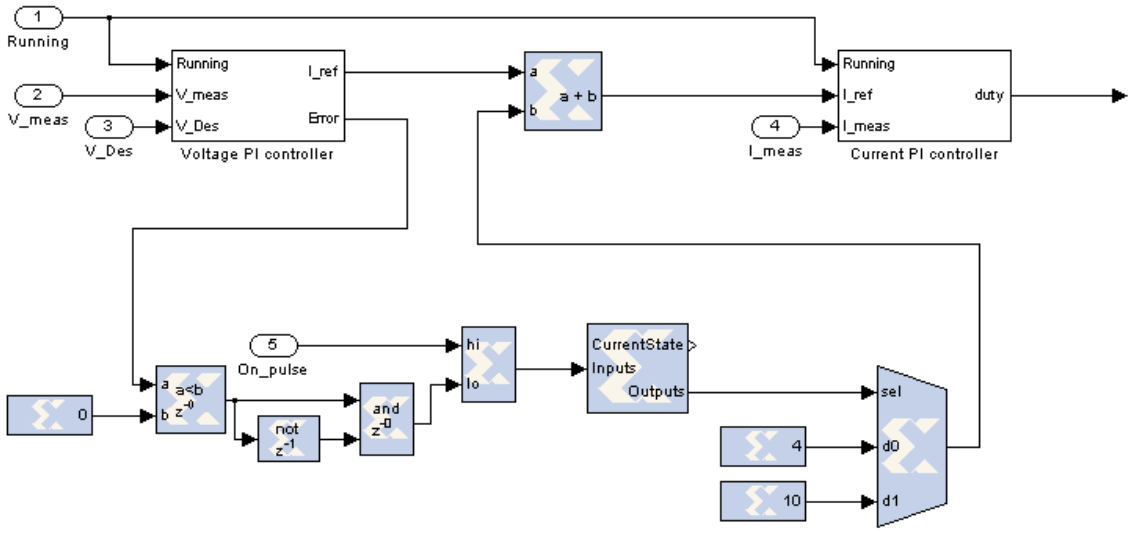

Figure 12. Control Scheme with Current Feed-Forward Terms

B. FAULT PROTECTION LOGIC

Fault protection logic is incorporated to ensure safe functionality of the device. A voltage protection is included to prevent the charger from exceeding voltage thresholds. A current limiter is used to prevent damage to the secondary diode rectifier. A time limiter is included to prevent the system from being on for longer than a desired time. Each of these protections shuts the converter off if a voltage, current, or time threshold is exceeded. Each signal is driven by the converter being turned on, and are ANDed together. Thus, the fault protection logic is active low. If the converter is running and none of the thresholds are exceeded, then the protection circuits each output a one to the AND gate. If one threshold is exceeded, the output of the protection logic goes low, and the "Running" signal that drives the converter goes low, and the converter shuts off. A simplified block diagram of this logic is shown in Figure 13. The three methods of protection are now discussed in detail.

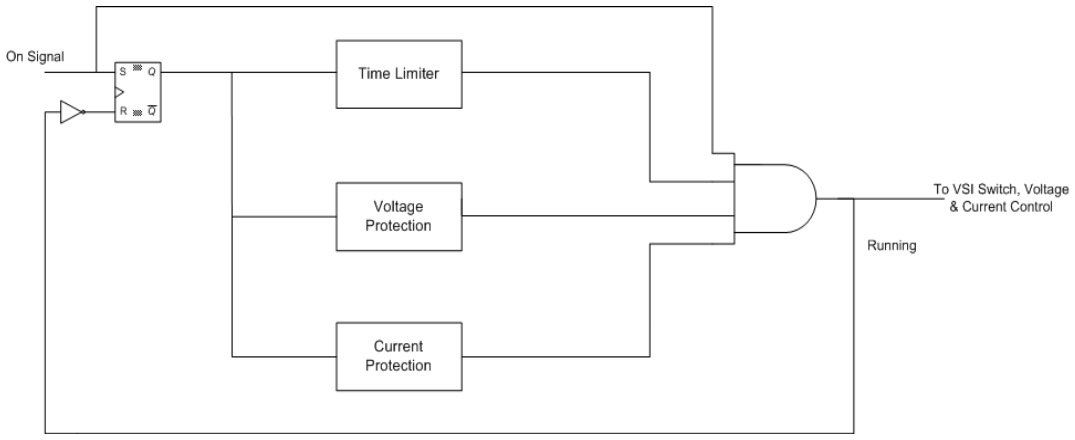

Figure 13. Block Diagram of Fault Protection Logic

1. Over Voltage Protection

Over voltage protection is achieved with a simple comparison test. The Xilinx blocks generating the code for this protection is are seen in Figure 14.

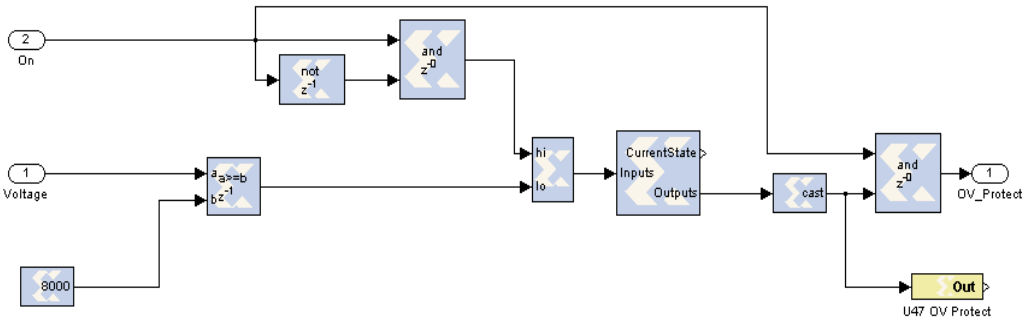

Figure 14. Over Voltage Protection Xilinx Blocks

The "on" signal sets an SR flip-flop, the output of which is ANDed with the on signal itself to ensure no false setting or resetting. If the threshold voltage is exceeded then the flip-flop is reset, and the signal "OV_Protect" goes low. This signal is then ANDed with the other protection signals, the output of which is the "Running" signal. The Out block labeled "U47 OV Protect" configures an output pin to a BNC port to as a test point to determine the fault source if the converter is shut off spuriously.

The SR flip-flop used is not part of the Xilinx blockset and works as follows. The output of the flip flop is a function of the current state and the inputs. The inputs are the values for S and R, and the current state is either 0 or one. For example, if the current state is 0 and the current value of the output is 0, and the input for S is 1 and R is 0, then the output will become 1, as seen above, and the next state will be state 1. As long as the R input bit is not a 1, the output will remain a 1, and the current state will remain one. The truth table for the SR flip flop is shown in Table 2. The SR inputs are under the columns S and R. In a Mealy state machine the next state depends on the current state, and the column "state" indicates the value of the current state. The next state of the state machine equals the output. This same flip flop is implemented throughout the converter control software.

S	R	State	Output
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Table 2. Truth Table for SR Flip Flop

2. Over Current Protection

Over current protection is implemented in a similar manner as the over voltage protection. The measured current value is compared to a threshold, and if the threshold is exceeded, the converter shuts off. Again, this logic is active low. The Xilinx block configuration that generates the code is seen in Figure 15. Note the similar configuration to the over voltage protection.

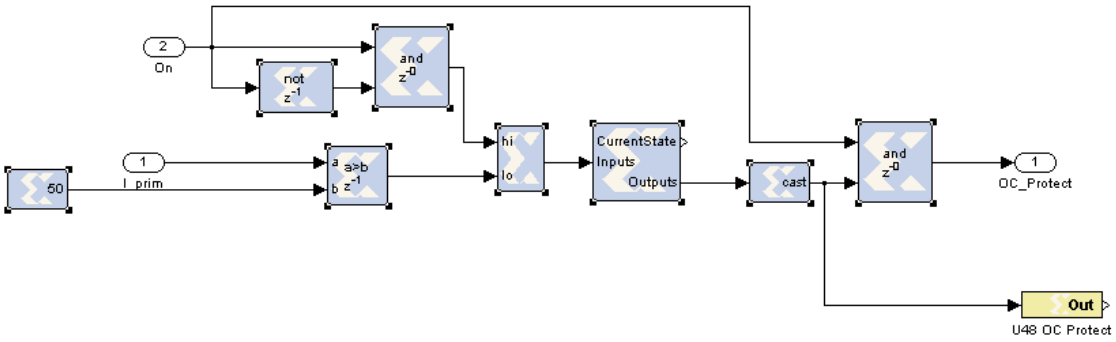

Figure 15. Over Current Protection Xilinx Blocks

3. Timer Shut Off

The switching of IGBTs generates a great deal of heat. The charging of the high voltage capacitor is completed quickly enough that overheating of the devices is generally not an issue. However, if the device were to be left on for an extended period

of time, the IGBTs would heat up to an undesirable temperature. To prevent this, a time limiter is implemented in the software. This timer shut off is implemented similarly to the voltage and current protection. A counter is started when the converter at the rising edge of an on pulse, which also sets an SR flip flop. With a 24 MHz clock (the FPGA clock), the counter counts to 24000000 in one second. With timer is set for five minutes, and $5\,\text{min}\left(\frac{60\,\text{sec}}{1\,\text{min}}\right)\left(\frac{24000000\,cycles}{1\,\text{sec}}\right)$=7200000000, the converter will shut off after 7200000000 clock cycles. Five minutes is a safe time preventing the IBGTs from overheating

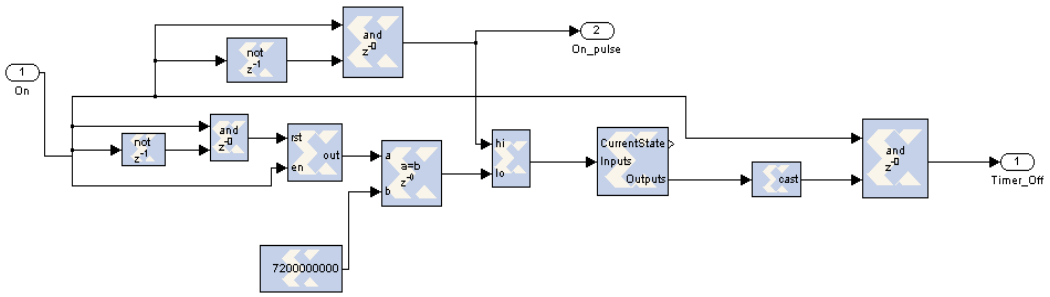

Figure 16. Timer Shut Off Xilinx Blocks

C. FIRING AND CHARGING CONTROL

A high level control mechanism in the Xilinx FPGA allows integration of charging and firing control. Control software is integrated in order to control turning the converter to begin charging; shutting off the converter to stop charging, and firing the capacitor. This control also uses a Xilinx Spartan III FPGA development board as a control panel for the user (now referred to as the Spartan board). The software used in the firing and charger control had been previously developed at NPS. This software can be divided into three sections; the first being the input from the Spartan board to the converter control board (now referred to as the Virtex board), the output from the Virtex board to the Spartan board; and the control software on the Spartan board. The Spartan board and the Virtex board are connected by fiber optic cable, to electrically isolate the operator from the high voltage equipment.

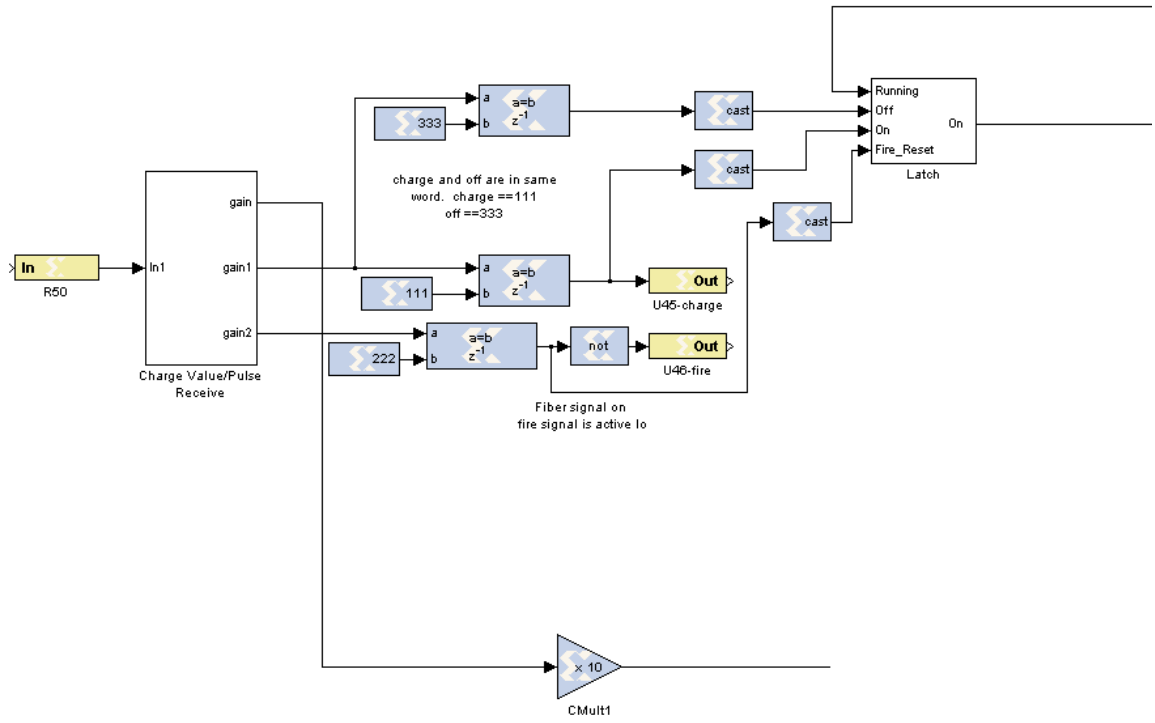

Figure 17. Fire and Control Input Software

Figure 17 shows the software decoding the input signal from the Spartan board to the Virtex board. The serial signal comes into the Virtex on pin R50, and is converted in the subsystem "Charge Value/Pulse Receive." The output of this subsystem has three values: gain, gain1 and gain2. The signal "gain" is the desired voltage signal selected by the user from the Spartan board. This value sent from the Spartan is multiplied by ten to reduce the size of the word containing the desired voltage value sent to the Virtex board. The signal is then sent to the voltage PI controller.

The signal "gain1" contains two possible values sent in the same word. One value (111) turns the charger on, and the other value (333) turns the charger off. On the Spartan board, two push buttons are set up as a charge button (or converter on) and an off (converter off) button. These two values are sent to the subsystem "Latch" to de-bounce and latch the pushing of the buttons, i.e. when the on button is on, the signal "on" stays on.

The signal “gain2” contains the word with the value (222) to fire the capacitor. This signal is sent out from the Spartan board, to the Virtex board, and from the Virtex board, by way of the U46 pin, to a thyristor gate driver circuit. The thyristor gate driver circuit controls thyristors that block the discharge of the capacitors.

The measured voltage across the capacitors is sent to the Spartan board by the software shown in Figure 18. The subsystem “Display Hold” holds the value of the capacitor voltage that is then divided by ten to enabling a transferable 12 bit word size to the Spartan board. The value is then displayed on the Spartan board. The subsystem “Serial_Encoder” serializes the voltage value sent to the Spartan board.

Figure 18. Fire and Control Output Software

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VI. RESULTS AND ANALYSIS

A. PROOF OF WORKING CONVERTER

The metric for a working converter is as follows. Acceptable voltage controller performance is charging of the high voltage capacitor to the desired voltage within 5% error. Acceptable current controller performance maintains the current at an average value below the acceptable value for the high voltage diode string. In addition, when the feed forward term is changed when the target voltage is reached the feed forward logic is working properly.

Transformer boosting is verified by comparing secondary and primary current waveforms. The boosting ratio of the transformer in the working converter is at or very near the boosting ratio determined in IV.B.

Proper fault protection occurs when the charger shuts off when reaching the threshold for voltage protection. The test point BNC is checked to see if the pin corresponding to the fault goes low. Correct operation of the current protection was determined in the same manner as the voltage protection.

The voltage controller reached a voltage of 8850 V when set to 9000 V, an error of only 1.7%, within the acceptable error range. The current controller maintains the average value of the current at approximately 220 mA during charging. The timer, over voltage, and over current fault protection each shut the charger off when thresholds were exceeded, shown by the test point BNCs.

B. CONVERTER WAVEFORMS

After the charger was determined working, measurements were taken to verify the converter's operation. Measurements were taken with an Agilent Infiniium 2.25 GHz oscilloscope. The data was then loaded and plotted in Matlab.

Figure 19 shows the capacitor step response for a desired voltage of 900 V. The capacitor was charged to higher voltages, but charging to 900 V is sufficient to show the

functionality of the capacitor charger and allows primary and secondary voltage and current measurements. Because of the feed forward control term added to the current reference, this step response has a linear appearance. The instant at which the feed forward term is removed is the point where the voltage suddenly flattens out, i.e. the capacitor reaches charge voltage.

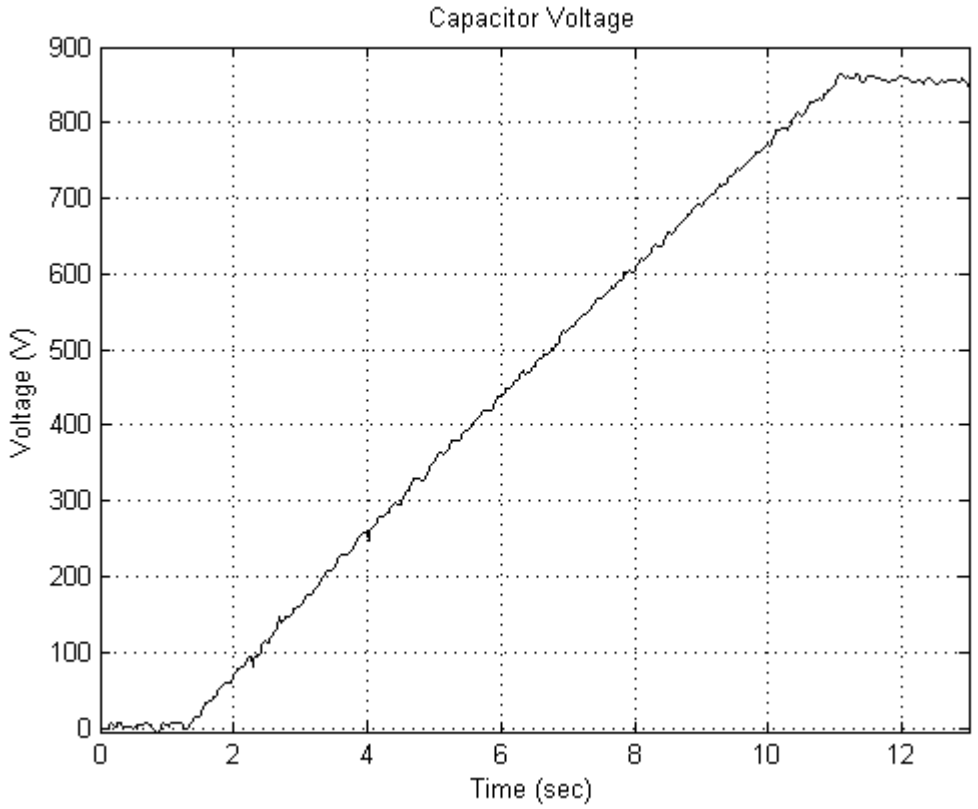

Figure 19. Capacitor Step Response

The primary and secondary current waveforms are also of interest. The two measurements taken were at the instant the converter was turned on and after the capacitor reached desired charge voltage. The measurement for the primary current was made at the output of the VSI with a current transformer (CT). The measurement for the secondary current was made at the output of the transformer, made with a different CT. Figure 20 shows four complete cycles of the primary current at the instant when the converter is turned on.

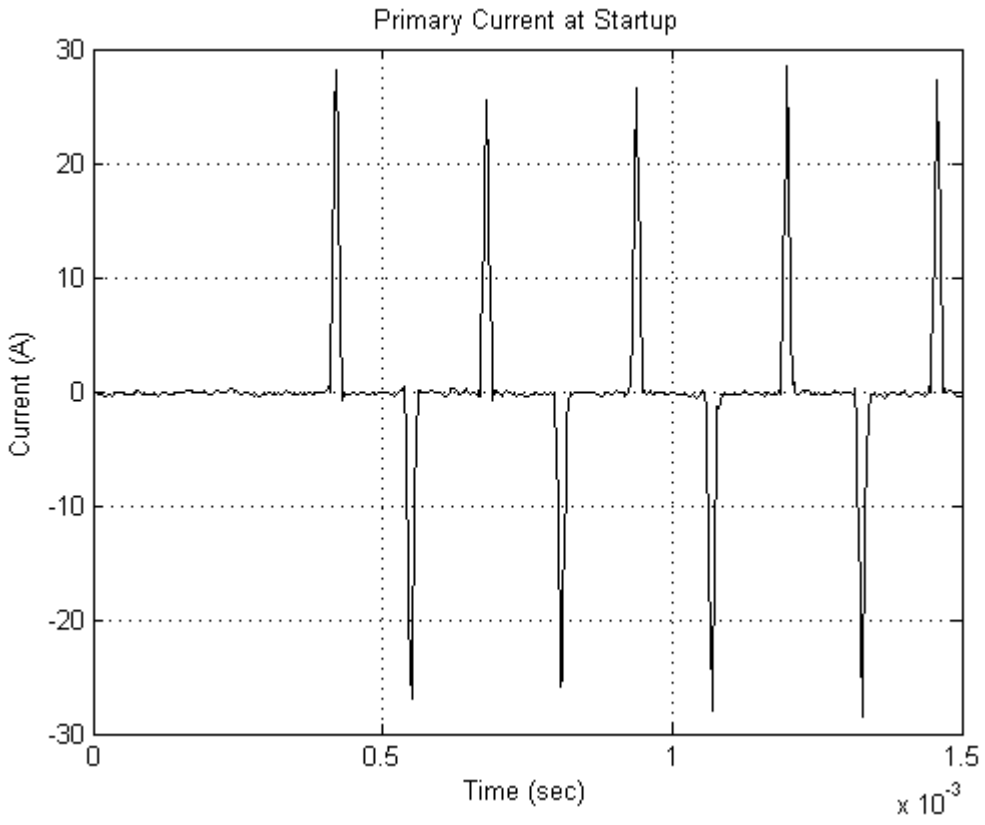

Figure 20. Primary Current at Startup

The secondary current was measured on the same charging cycle startup as the primary current measurement. Figure 21 shows the same cycles on the secondary current as the primary cycles in Figure 20. The max peak current value in the primary current in Figure 20 is 28.48 A. The max peak current value in the secondary current in Figure 21 is 2.33 A. The transformer is bucking the current by a factor of 12.2. The frequency of the switching period can be measured at 4 kHz. Note that the converter is operating in discontinuous conduction mode.

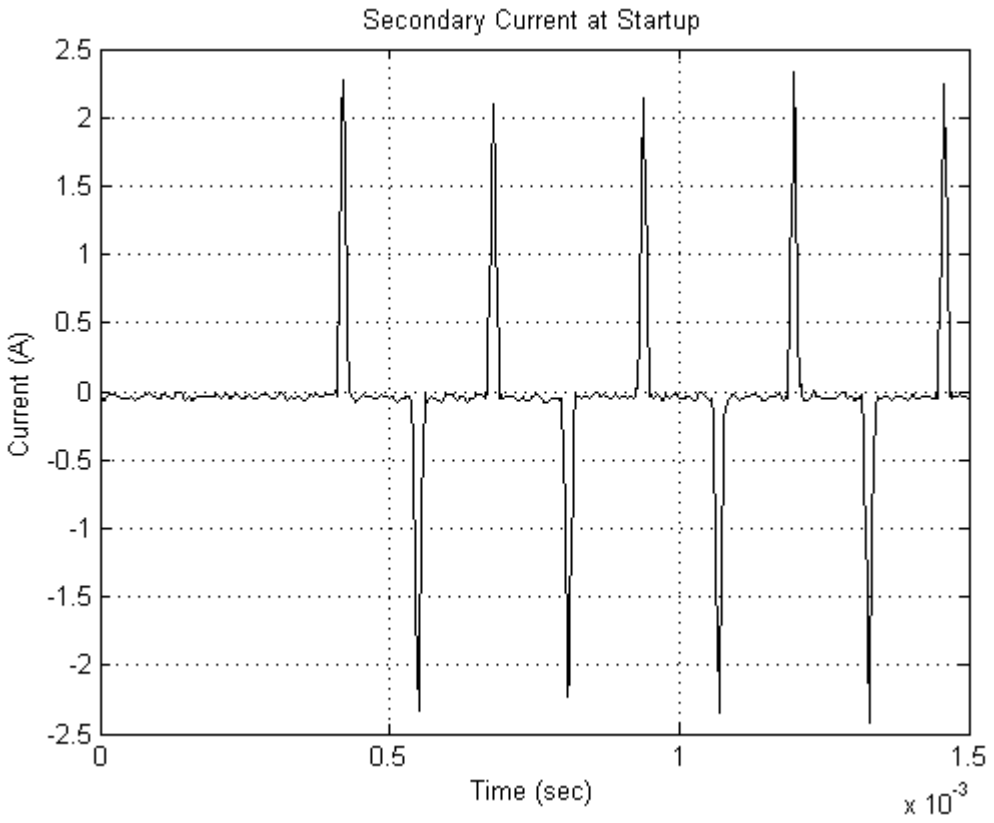

Figure 21. Secondary Current at Startup

After reaching the target voltage, the feed forward term on the current controller is removed, and the peaks of the current pulses drop considerably. The current pulses are still present, fighting the leakage current of the thyristors, maintaining the desired voltage across the capacitor. The peak current in Figure 22 is 5.21 A, and in Figure 23 the peak value is 0.4515 A.

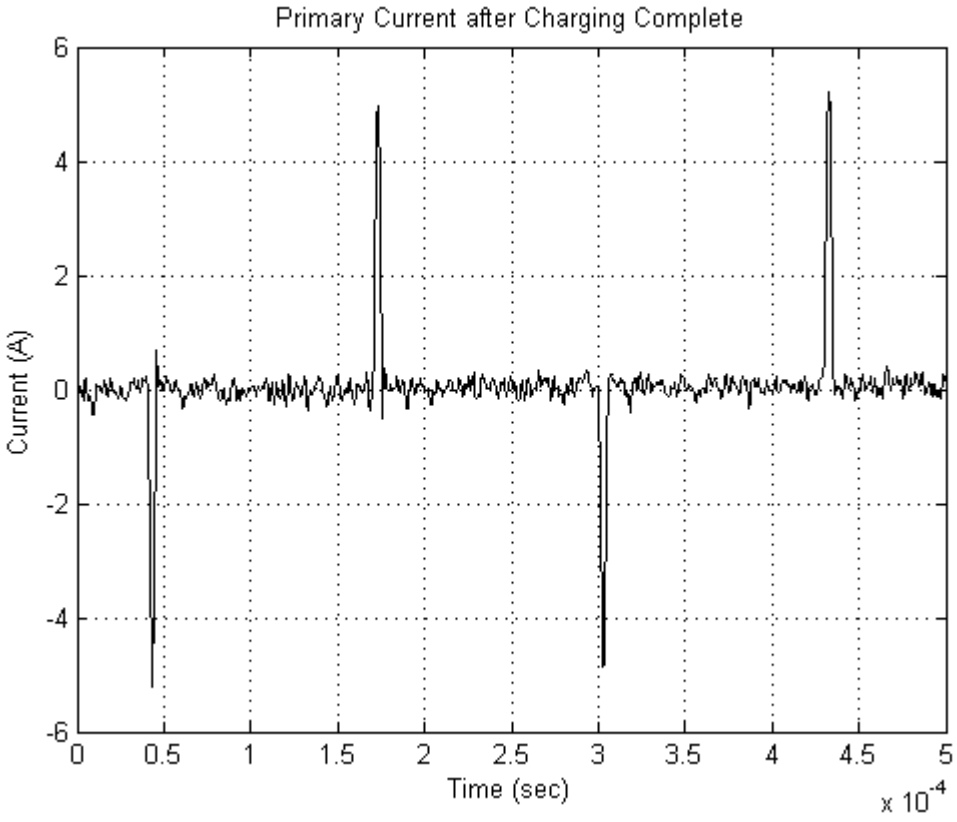

Figure 22. Primary Current After Reaching Target Voltage

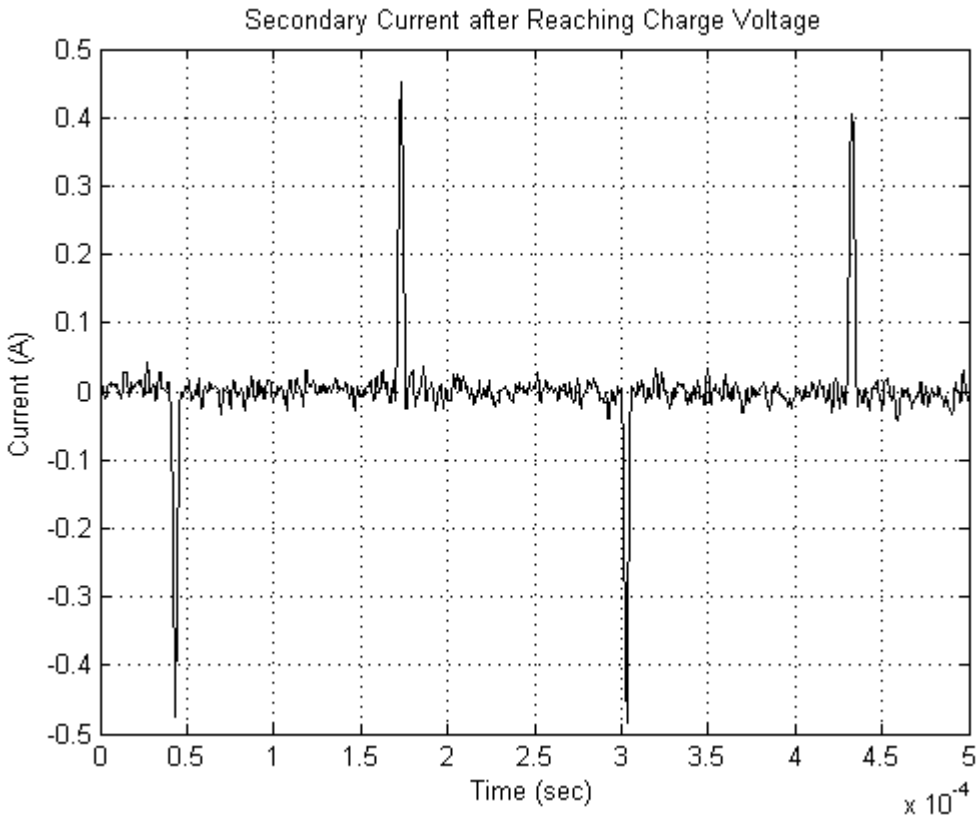

Figure 23. Secondary Current After Reaching Target Voltage

Converter voltage waveforms also bear relevance at this point. Measurements were taken at the same time as the current waveforms; at startup and after reaching charge voltage. Voltage measurements were taken with an additional Tektronix P2500 High Voltage Probe and measured on an Agilent Infiniium 2.25 GHz oscilloscope. Because of the configuration of the converter, it is not possible to take primary voltage measurements. The secondary voltage at startup and after charging is complete can be seen in Figure 24 and Figure 21 respectively. Note that the voltage at the output of the transformer starts at a much lower voltage than the DC bus voltage multiplied by the turns ratio. The capacitors in the high voltage doubler rectifier are charging up to half of the desired output voltage.

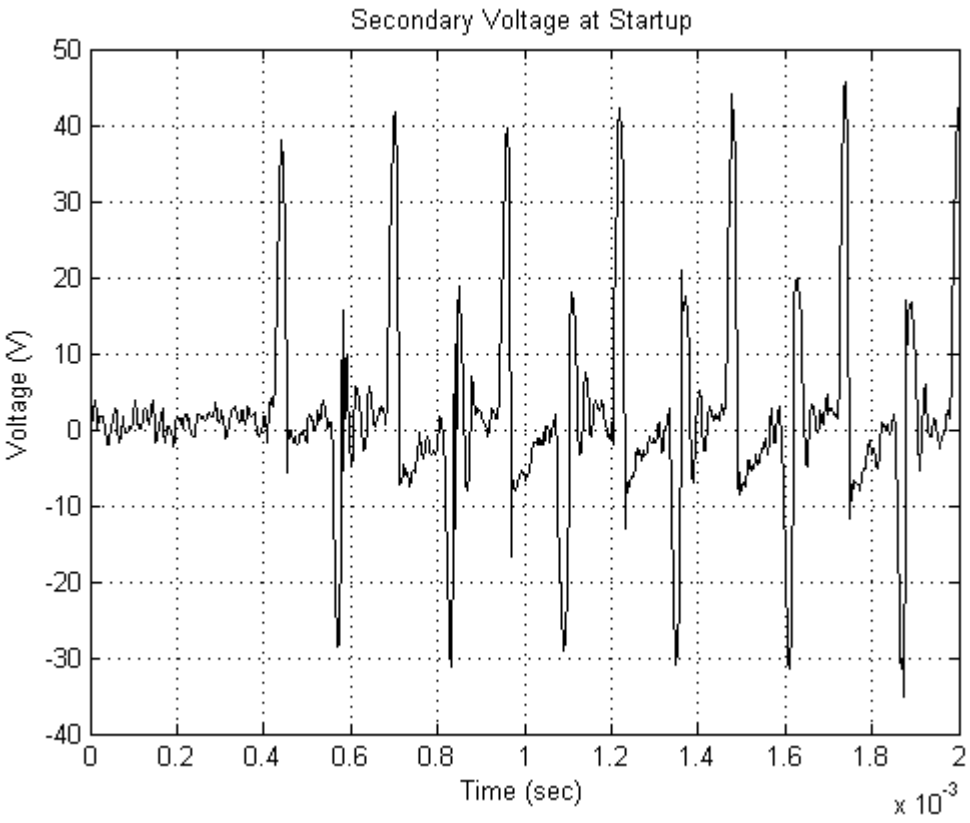

Figure 24. Secondary Voltage Waveform at Startup

Figure 24 shows the secondary voltage at startup measured at the output of the transformer. When an IGBT in the H-Bridge turns on, the capacitors in the high voltage doubler rectifier begin to charge. The voltage peaks get larger as the capacitor charges on both the negative and positive pulses. When the IGBT turns off, there is an LC oscillation due to the parasitic capacitance in the string of diodes and the inductance in the secondary of the transformer. This oscillation decays to zero before an IGBT is switched on again.

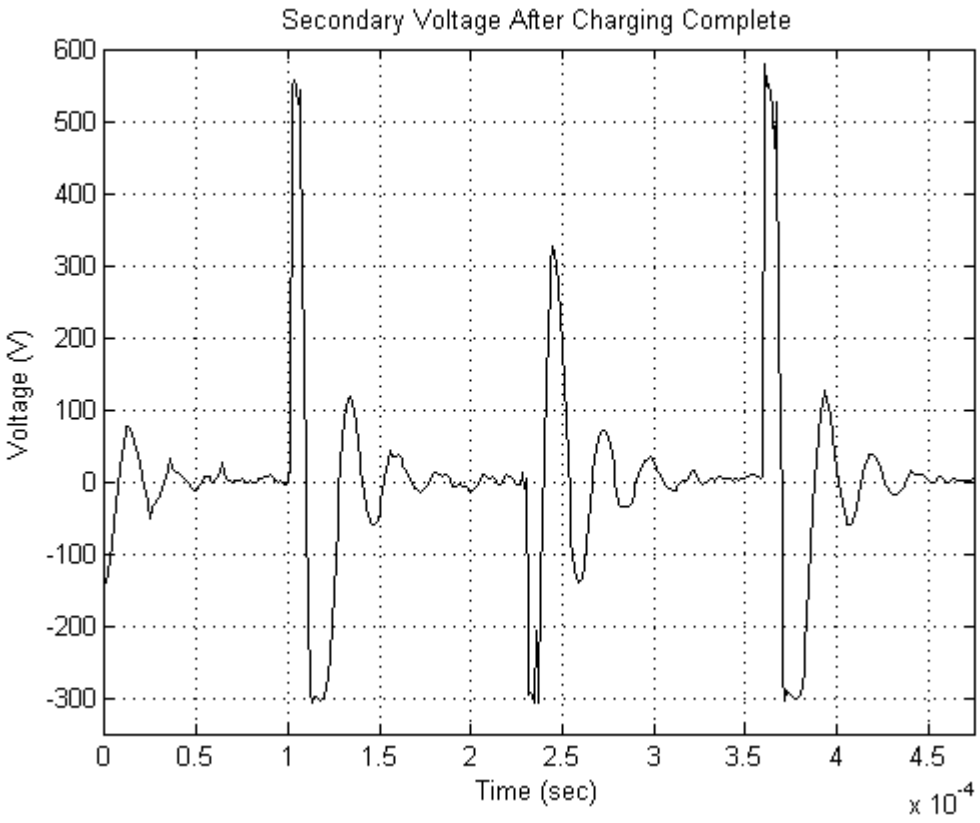

Figure 25. Secondary Voltage After Charging Complete

Figure 25 shows the secondary voltage at the output of the transformer after charging is complete. On the positive pulse the voltage goes to approximately 580 V. On the negative pulse the voltage peaks at -300 V. The difference between these two values is approximately the desired charge voltage of 900 V. The oscillation after the switch turns off is caused by the LC circuit created by the inductance of the secondary transformer windings and the parasitic capacitance in the diodes when blocking current. This oscillation dies out before the converter is switched on again.

C. WAVEFORM COMPARISON (SIMULATION/ACTUAL)

Comparing the simulated waveforms to the actual waveforms collected illustrates the usefulness of physics based modeling in design. The main goal of using the simulation was to select parts, predict operation, and tune the converter controller.

The simulation used is discussed in III.B. One important change is made regarding current measurement. The Hall Effect sensor used to measure the primary current has a limited bandwidth; the A/D converter also samples and holds the value of the current. These characteristics affected the control calculations a great deal. To account for these non-linearities, additional elements were added to the simulation. A low pass filter was added to the current measurement to account for bandwidth limitations. A transport delay was added to simulate the sample and hold of the A/D converter.

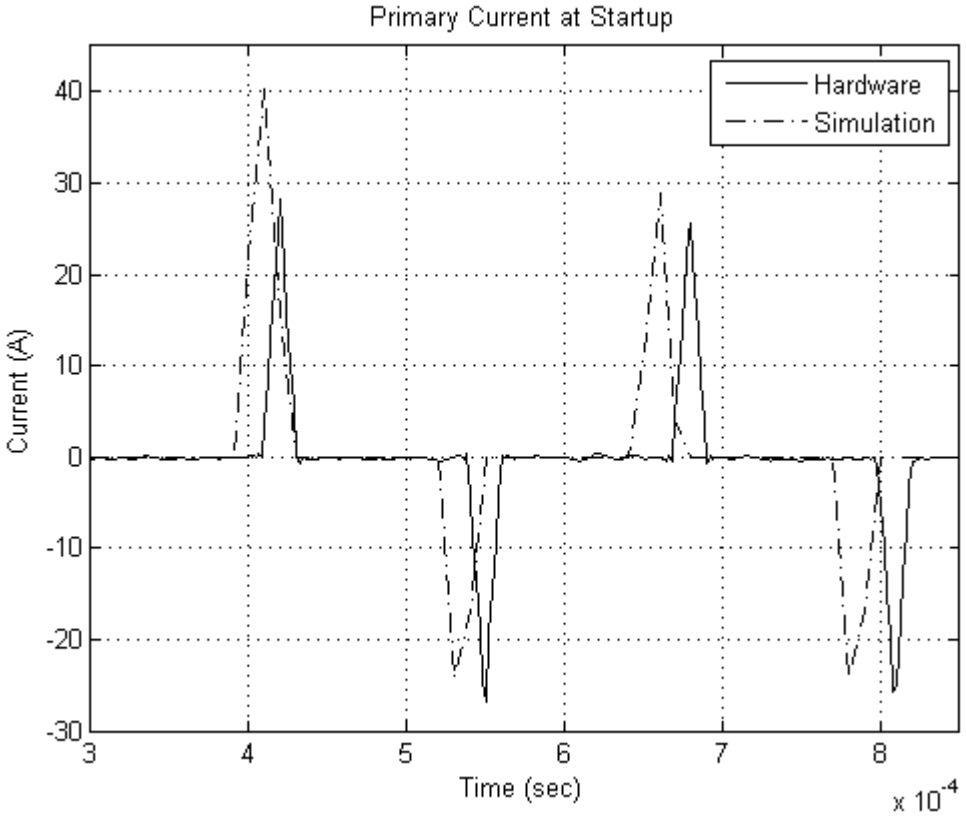

Figure 26. Primary Current Comparison at Startup

Figure 26 shows the comparison between the primary current in the hardware and the primary current in the simulation at startup. At first glance the waveforms seem quite similar. Note that there is some difference in the peaks of the current pulses. Peak value for the hardware is 28.48 A. The peak (not including the initial starting peak) in the simulation current waveforms is 31.43 A, an error of about 10%.

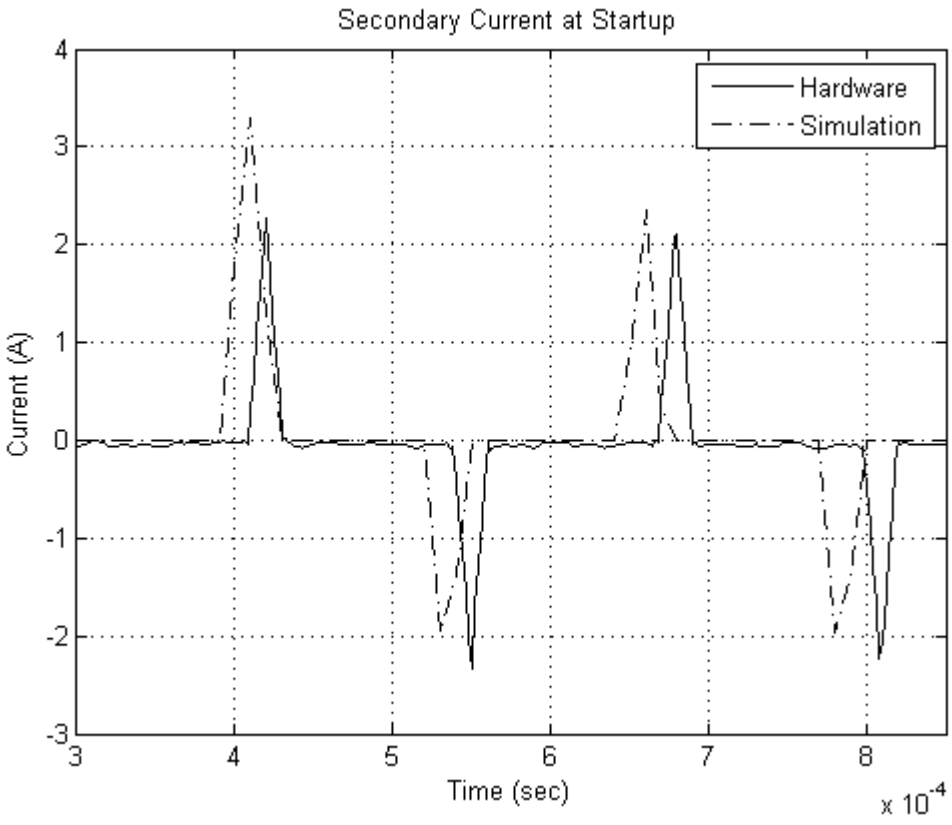

Figure 27. Secondary Current Comparison at Startup

Figure 27 shows a comparison of the secondary currents at startup. The peak value for the simulation current is 2.57 A. The peak value in the hardware is 2.33 A; yielding about a 10% difference between simulation and measured values.

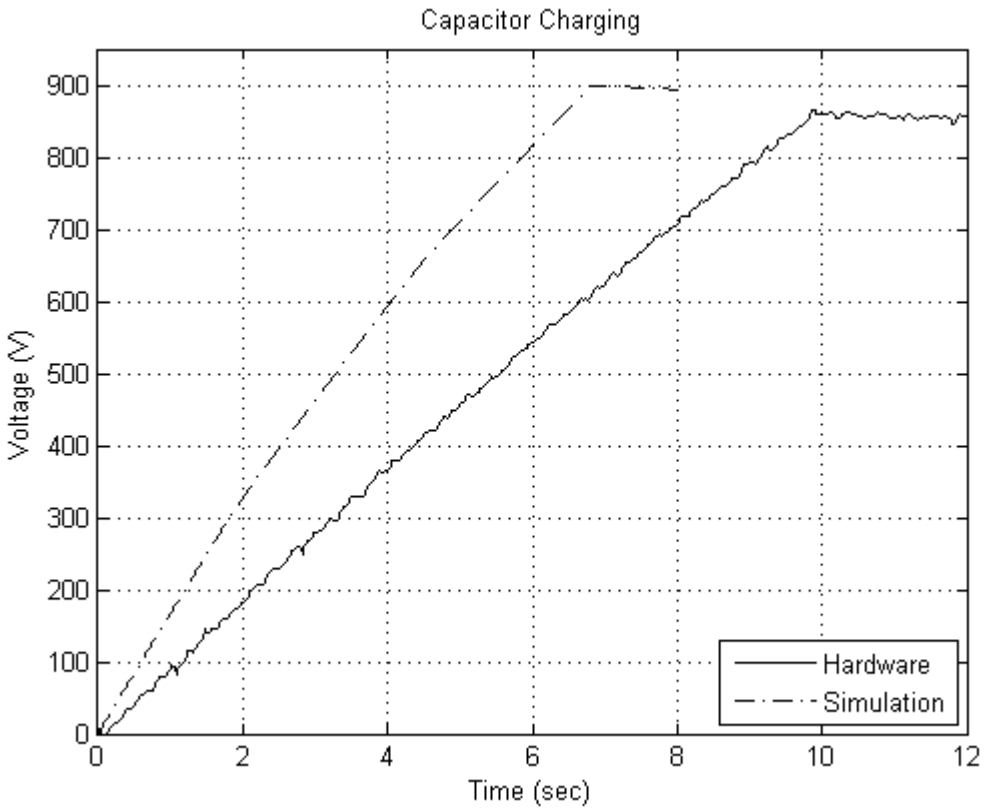

Figure 28. Capacitor Charging Comparison

Figure 28 shows a comparison between the actual capacitor charging and the simulation capacitor charging. Note the difference in time between the two capacitors. The actual capacitor charges in about 9.7 seconds, where the simulation capacitor charges in about 6.7 seconds. This difference is due to the higher current peaks in simulation than in actual charging, as seen in Figures 26 and 27.

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VII. CONCLUSIONS AND SUGGESTIONS

A. CONCLUSIONS

The power supply was tested to a voltage of 8850 V. This is an error of 1.7% from a desired voltage set point of 9000 V, within the acceptable range or error presented in the metric. It may be possible that higher voltages can be reached with this charger. However, the lifetime of the capacitor declines exponentially as the voltage approaches 11 kV. Thus reaching a charge voltage near 9000 V suffices for the current railgun program.

Successful charger operation demonstrates the benefit of designing and constructing a capacitor charger with the aid of simulation. The charger successfully and repeatedly charges a high voltage capacitor to desired voltages.

B. SUGGESTIONS FOR FURTHER RESEARCH

A wide variety of possibilities exist for further research in railgun power supplies. Limiting the suggestions to this configuration of solid state power supply is necessary for an effective focus of this thesis.

Further research on the charging supply controller can be done to tune the PI controller gains to an optimal selection across all desired voltages. There is opportunity to research accurate high voltage sensing and measurements for this application. In the area of sensor research, reducing the number of sensors (getting the voltage observer working) is a definite area of research possibility. Redesigning the charger supply to size and performance is an additional area of research. Additional study in the area of power converter simulation is an effective study that can better aid in examining changes to converter design.

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APPENDIX DATASHEETS

This appendix contains the data sheets for major components used in the capacitor charger. The LPT40 is the power supply for the IGBT gate drivers, the Virtex2 control board, and the firing and control cards.

40 Watts
LPT40 Series

Total Power: **40-55 Watts**
Input Voltage: **85-264 VAC**
120-300 VDC
# of Outputs: **Triple**

Special Features

- Universal input
- 3" x 5" footprint
- Remote sense on main output
- Built-in EMI filter
- Low output ripple
- Adjustable main output
- Overvoltage protection
- Overload protection
- 110 KHz switching frequency
- LPX40 enclosure kit available

Environmental

Operating temperature: 0° to 50°C ambient; derate each output at 2.5% per degree from 50° to 70°C

Electromagnetic susceptibility: designed to meet IEC 801, -2, -3, -4, -5, -6, Level 3

Humidity: Operating: non-condensing 5% to 95%

Vibration: Three orthogonal axes, sweep at 1 oct/min, 5 min. dwell at four major resonances 0.75 G peak 5 Hz to 500 Hz, operational

Storage temperature: -40° to 85°C

Temperature coefficient: ±.04% per °C

MTBF demonstrated: >550,000 hours at full load and 25°C ambient condition

Electrical Specs

Input	
Input range	85-264 VAC 120-300 VDC
Frequency	47-440 Hz
Inrush current	<18 A peak @ 115 VAC; <36 A peak @ 230 VAC, cold start @ 25°C
Input current	1 A max. (RMS) @ 115 VAC
Efficiency	70% typical at full load (60% for LPT41)
EMI filter	FCC Class B conducted CISPR 22 Class B conducted EN55022 Class B conducted VDE 0878 PT3 Class B conducted
Safety ground leakage current	<0.5 mA @ 50/60 Hz, 264 VAC input
Output	
Maximum power	40 W for convection, (LPT41, 25W); 55 W with 30 CFM forced air (LPT41, 41W)
Adjustment range	-5, +10% minimum
Cross regulation	±2% on output 1; ±5% on outputs 2, 3
Hold-up time	20 ms @ 40 W load, 115 VAC nominal line
Overload protection	Short circuit protection on all outputs. Case overload protected @ 110-145% above peak rating
Overvoltage protection	5.7 to 6.7 VDC on main output LPT41: 3.6 to 4.6 VDC
Remote sense	Compensates for 0.5 V lead drop min. Will operate without remote sense connected. Reverse connection protected.

Safety

VDE	0805/EN60950 (IEC950)	11774-3336-1241 (LC# 84936)
UL	UL1950	E132002
CSA	CSA 22.2-234 Level 3	LR53982C
NEMKO	EN 60950/EMKO-TUE (74-sec) 203	P94100374
BABT	EN60950/BS7002	PS/604782
CB	Certificate and report	1118,1122,1123,1124
CE	Mark (LVD)	

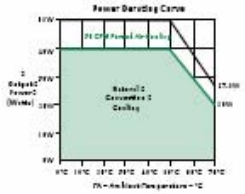
Ordering Information

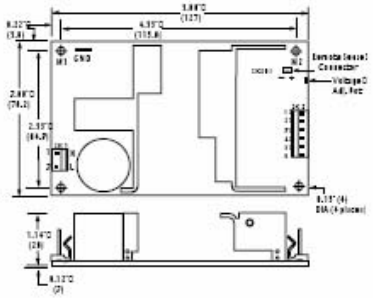
Model Number	Output Voltage	Minimum Load	Maximum Load with Convection Cooling	Maximum Load with 30 CFM Forced Air	Peak Load1	Regulation2	Ripple P/P (PARD)3
LPT41	+3.3 V	0.5 A	4 A	7 A	7 A	±2%	50 mV
	+5 V	0	1.5 A	2.0 A	2.5 A	±2%	50 mV
	+12 V	0	0.5 A	0.7 A	0.7 A	±5%	120 mV
LPT42	+5 V	0.4 A	4 A	5 A	7 A	±2%	50 mV
	+12 V	0.2 A	2 A	2.5 A	4 A	±5%	120 mV
	-12 V	0 A	0.5 A	0.7 A	1 A	±5%	120 mV
LPT43	+5 V	0.5 A	6 A	8 A	9 A	±2%	50 mV
	+12 V	0 A	0.5 A	0.7 A	1 A	±5%	120 mV
	-12 V	0 A	0.5 A	0.7 A	1 A	±5%	120 mV
LPT44	+5 V	0.4 A	4 A	5 A	7 A	±2%	50 mV
	+12 V	0.2 A	2 A	2.5 A	4 A	±5%	120 mV
	-5 V	0 A	0.5 A	0.7 A	1 A	±5%	50 mV
LPT45	+5 V	0.4 A	4 A	5 A	7 A	±2%	50 mV
	+15 V	0.2 A	2 A	2.5 A	3 A	±5%	150 mV
	-15 V	0 A	0.5 A	0.7 A	1 A	±5%	150 mV
LPT46	+5 V	0.4 A	4 A	5 A	6 A	±2%	50 mV
	+24 V	0.1 A	1.0 A	1.5 A	2 A	±7%	240 mV
	+12 V	0 A	0.5 A	0.7 A	1 A	±5%	120 mV
LPT47	+5 V	0.4 A	4 A	5 A	6 A	±2%	50 mV
	+24 V	0.2 A	1.0 A	1.5 A	2 A	±7%	240 mV
	-12 V	0 A	0.5 A	0.7 A	1 A	±5%	120 mV

1. Peak current lasting <20 seconds with a maximum 10% duty cycle.
2. At 25°C including initial tolerance, line voltage, load currents and output voltages adjusted to factory settings.
3. Peak-to-peak with 20 MHz bandwidth and 10 µF in parallel with a 0.1 µF capacitor at rated line voltage and load ranges.
4. Minimum Loads are required.

Pin Assignments

Connector	LPT41	LPT42	LPT43	LPT44	LPT45	LPT46	LPT47
SK1-1	Neutral	Neutral	Neutral	Neutral	Neutral	Neutral	Neutral
SK1-2	Line	Line	Line	Line	Line	Line	Line
SK2-1	3 V	+12 V	+12 V	+12 V	+15 V	+24 V	+24 V
SK2-2	3.3 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V
SK2-3	3.3 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V
SK2-4	Common	Common	Common	Common	Common	Common	Common
SK2-5	Common	Common	Common	Common	Common	Common	Common
SK2-6	12 V	-12 V	-12 V	-5 V	-15 V	+12 V	-12 V
SK201-1	+Sense	+Sense	+Sense	+Sense	+Sense	+Sense	+Sense
SK201-2	-Sense	-Sense	-Sense	-Sense	-Sense	-Sense	-Sense





Mating Connectors

AC Input: Molex 09-50-8031 (USA)
09-91-0300 (UK)
PINS: 08-50-0111

DC Outputs: Molex 09-50-8061 (USA)
09-91-0600 (UK)
PINS: 08-50-0111

Remote Sense: Molex 22-01-2025
PINS: 08-50-0114

Astec Connector Kit #70-841-006, includes all of the above.

Notes:

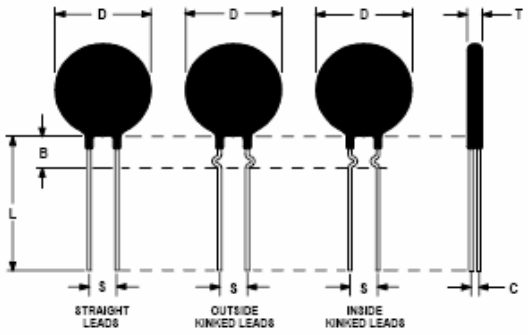
1. Specifications subject to change without notice.
2. All dimensions in inches (mm), tolerance is ±.02".
3. Mounting holes M1 and M2 should be grounded for EMI purposes.
4. Mounting hole M1 is safety ground connection.
5. Specifications are for convection rating at factory settings at 115 VAC input, 25°C unless otherwise stated.
6. Warranty: 1 year
7. Weight: 0.5 lb. / 0.23 kg

The Ametherm Circuit Protection Thermistors are placed in the AC 208 V_{rms} supply line before the DC bus to limit the inrush current to the capacitors.

AMETHERM
Circuit Protection Thermistors

DATA SHEET

Part Number: MS35 3R030



Electrical Specifications:

Resistance @ 25°C	3.0 Ω
Max Steady State Current Up to 65°C	30.0 A
Max Recommended Energy Rating (Joules)	750.0 J
Rhot @ 100% Steady State Current	0.030 Ω
Rhot @ 75% Steady State Current	0.040 Ω
Rhot @ 50% Steady State Current	0.065 Ω
Rhot @ 25% Steady State Current	0.155 Ω
Max Capacitance @ Max Voltage	1600 µF
Max Recommended Voltage	680 V
Material Type	"C"

Mechanical Specifications:

D	35.0 ± 2.5 mm
T	10.0 ± 2.0 mm
Lead Diameter	2.5 ± 0.1 mm
S	19.0 ± 3.0 mm
L	39.0 ± 4.0 mm
Straight Leads Coating Run Down	9.0 mm Max
B	25.0 ± 2.5 mm
C	7.50 ± 1.0 mm

Revision Date: March 19, 2003

Ametherm, Inc. 3111 N. Deer Run Road #4 Carson City, NV 89701
Telephone: (800) 808-2434 (775) 884-2434 Fax: (775) 884-0670
www.ametherm.com

The SEMISTACK SEMITEACH is a three phase rectifier and inverter. This device is used as the low voltage doubler rectifier and the VSI.

SEMISTACK - IGBT

SEMITRANS Stack[1)]

Three-phase rectifier + inverter with brake chopper

SEMITEACH - IGBT
SKM 50 GB 123D
SKD 51
P3/250F

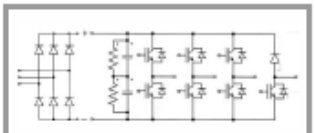
Features

- Multi-function IGBT converter
- Transparent enclosure to allow visualization of every part
- IP2x protection to minimize safety hazards
- External banana/BNC type connectors for all devices
- Integrated drive unit offering short-circuit detection/cut-off, power supply failure detection, interlock of IGBTs + galvanic isolation of the user
- Forced-air cooled heatsink

Typical Applications

- Education: One stack can simulate almost all existing industrial applications:
- 3-phase inverter+brake chopper
- Buck or boost converter
- Single phase inverter
- Single or 3-phase rectifier

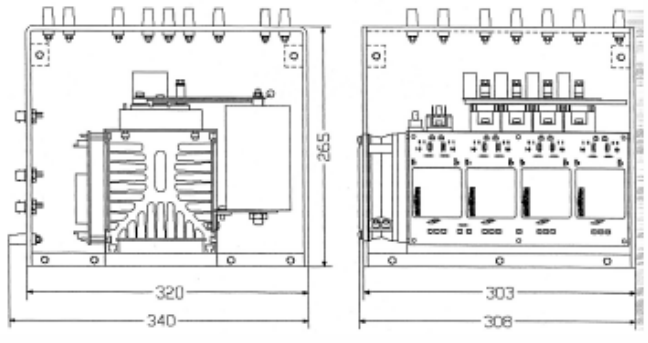
[1)] Photo non-contractual



B6U + B6CI + E1CIKF

Circuit	I_{rms} (A)	V_{ac} / V_{dcmax}	Types
B6CI	30	440 / 750	SEMITEACH - IGBT

Symbol	Conditions	Values	Units
I_{rms}	no overload	30	A
	IGBT - 4x SKM 50 GB 123D		
V_{CES}		1200	V
$V_{CE(SAT)}$	I_C= 50A, V_{GE}= 15V, chip level; T_j= 25(125)°C	2,7 (3,5)	V
V_{GES}		±20	V
I_C	T_{case}= 25 (80)°C	50 (40)	A
I_{CM}	T_{case}= 25 (80)°C; t_p= 1ms	100 (80)	A
	Rectifier - 1x SKD 51/14		
$V_{In(max)}$	without filter	3 x 480	V
	with filter	3 x 380	V
	DC Capacitor bank - Electrolytic 2x 2200µF/400V		
C_{eqM}	total equivalent capacitance	1100 / 800	µF / V
V_{DCmax}	max. DC voltage applied to the capacitor bank	750	V
	Driver - 4x SKHI 22		
Power supply		0 / 15	V
Current consumption	max; per driver	16	mA
Thermal trip	Normally Open type (NO)	71	°C



General dimensions

This technical information specifies semiconductor devices but promises no characteristics. No warranty or guarantee expressed or implied is made regarding delivery, performance or suitability.

This LEM Current Transducer is used to measure the primary current in the current control loop.

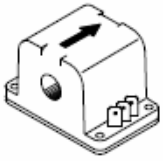
LEM

Current Transducer LT 100-S/SP30

I_{PN} = 100 A

For the electronic measurement of currents : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).

16240



Electrical data

I_{PN}	Primary nominal r.m.s. current		100		A
I_P	Primary current, measuring range		0 .. ± 200		A
R_M	Measuring resistance		$R_{M\,min}$	$R_{M\,max}$	
	with ± 12 V	@ ± 100 A_{max}	0	75	Ω
		@ ± 200 A_{max}	0	25	Ω
	with ± 18 V	@ ± 100 A_{max}	30	135	Ω
		@ ± 200 A_{max}	30	55	Ω
I_{SN}	Secondary nominal r.m.s. current		100		mA
K_N	Conversion ratio		1 : 1000		
V_C	Supply voltage (± 5 %)		± 12 .. 18		V
I_C	Current consumption		28 (@ ± 18 V) + I_S		mA
V_d	R.m.s. voltage for AC isolation test, 50 Hz, 1 mn		5		kV

Accuracy - Dynamic performance data

X_G	Overall accuracy @ I_{PN}, T_A = 25°C		± 0.5		%
ε_L	Linearity error		< 0.1		%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.4	mA
I_{OT}	Thermal drift of I_O	- 25°C .. + 70°C	± 0.3	± 0.6	mA
		- 40°C .. - 25°C	± 0.4	± 1.0	mA
t_r	Response time [1] @ 90 % of I_{PN}		< 1		µs
di/dt	di/dt accurately followed		> 50		A/µs
f	Frequency bandwidth (- 1 dB)		DC .. 150		kHz

General data

T_A	Ambient operating temperature		- 40 .. + 70	°C
T_S	Ambient storage temperature		- 50 .. + 85	°C
R_S	Secondary coil resistance @ T_A = 70°C		25	Ω
m	Mass		184	g
	Standards		EN 50155	

Note : [1] With a di/dt of 100 A/µs.

Features

- Closed loop (compensated) current transducer using the Hall effect
- Insulated plastic case recognized according to UL 94-V0.

Special features

- T_A = - 40°C .. + 70°C
- Potted.

Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

Applications

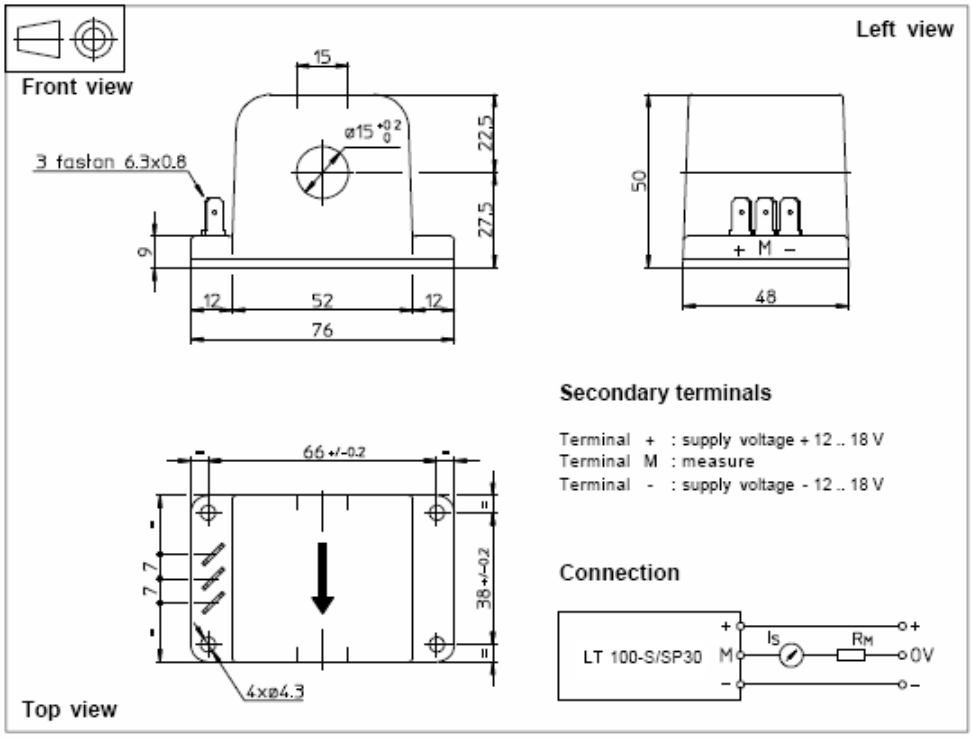
- Single or three phases inverter
- Propulsion and braking chopper
- Propulsion converter
- Auxiliary converter
- Battery charger.

Application domain

- Traction.

LEM reserves the right to carry out modifications on its transducers, in order to improve them, without previous notice.

Dimensions LT 100-S/SP30 (in mm. 1 mm = 0.0394 inch)



Secondary terminals

Terminal + : supply voltage + 12 .. 18 V
Terminal M : measure
Terminal - : supply voltage - 12 .. 18 V

Connection

Mechanical characteristics

• General tolerance	± 0.5 mm
• Transducer fastening	4 holes ∅ 4.3 mm 4 M4 steel screws
Recommended fastening torque	3.2 Nm or 2.36 Lb.-Ft.
• Connection of primary	∅ 15 mm
• Connection of secondary	Faston 6.3 x 0.8 mm

Remarks

- I_s is positive when I_p flows in the direction of the arrow.
- Temperature of the primary conductor should not exceed 100°C.

Safety

This transducer must be used in electric/electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions.

Caution, risk of electrical shock

When operating the transducer, certain parts of the module can carry hazardous voltage (eg. primary busbar, power supply). Ignoring this warning can lead to injury and/or cause serious damage.
This transducer is a built-in device, whose conducting parts must be inaccessible after installation.
A protective housing or additional shield could be used.
Main supply must be able to be disconnected.

LEM reserves the right to carry out modifications on its transducers, in order to improve them, without previous notice.

The Ohmite Supermox and Dale RS-10 high wattage resistors are used in the voltage divider circuit for the voltage probe.

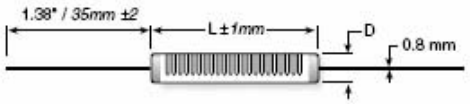
Super Mox Series

High Voltage

RoHS Compliant

High-voltage Super Mox resistors have been developed to meet the precision temperature stability requirements of high-accuracy and high-voltage systems. Super Mox combines proprietary non-inductive resistance system and design to achieve low temperature coefficient, low voltage coefficients, high stability and increased high operating voltages. These resistors are designed to meet the demanding requirements of high voltage power supplies, electron microscopes, X-ray systems, high resolution CRT displays and geophysical instruments.

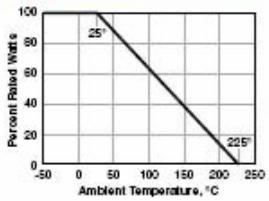
Uncoated resistor element pictured for demonstration purposes only. Finished product is coated with silicone.



SPECIFICATIONS

Resistance Range: from 1KΩ to 50GΩ on all models (contact Ohmite for 51G to 1TΩ)
Tolerances: 0.05%, 0.1%, 0.25%, 0.5%, 1%, 2%, 5%, 10% (0.05% avail. to 10G, 0.25% to 100G, other on request)
Temperature Coefficients: 5, 10, 15, 25, 50 and 100ppm/°C (10ppm/°C available to 10G, 25ppm/°C to 100G, other on request
Encapsulation: Silicone Conformal Coating
Terminal Material: Gold Plated
Core Material: Al_2O_3 (96%)
Resistor Material: Ruthenium Oxide
Operating Temperature: -55°C to 225°C (extended temperature range to 350°C available)

DERATING



PERFORMANCE DATA

Insulation Resistance	>10,000 MΩ	500 Volt 25 °C 75% relative humidity
Dielectric Strength	>1,000 Volt	25 °C 75% relative humidity
Thermal Shock	Δ R/R < 0.1% typ., 0.20% max.	MIL Std. 202, method 107 Cond. C (IEC 68 -2 -14)
Overload	Δ R/R < 0.1% typ., 0.25% max.	1.5 x Prorm, 5 sec (do not exceed max. voltage)
Moisture Resistance	Δ R/R < 0.1% typ., 0.25% max.	MIL Std. 202, method 106 (IEC 68 -2 -3)
Load Life	Δ R/R < 0.1% typ., 0.25% max.	1000 hours at rated power (IEC 115 -1)

STANDARD PART NUMBERS

Part Number	Watts	Ohms 1% tol.	TCR
MOX91021004FVE	3.8W	1M	50ppm
MOX91025004FVE	3.8W	5M	50ppm
MOX91021005FVE	3.8W	10M	50ppm
MOX91022505FTE	3.8W	25M	100ppm
MOX92021005FVE	5W	10M	50ppm
MOX92025005FVE	5W	50M	50ppm
MOX92021006FVE	5W	100M	50ppm
MOX92021007FTE	5W	1000M	100ppm
MOX93021004FVE	7.5W	1M	50ppm
MOX93025004FVE	7.5W	5M	50ppm
MOX93021005FVE	7.5W	10M	50ppm
MOX93022505FTE	7.5W	25M	100ppm
MOX94021005FVE	10W	10M	50ppm
MOX94025005FVE	10W	50M	50ppm
MOX94021006FVE	10W	100M	50ppm
MOX94021007FTE	10W	1000M	100ppm
MOX95021004FVE	13.5W	1M	50ppm
MOX95025004FVE	13.5W	5M	50ppm
MOX95021005FVE	13.5W	10M	50ppm
MOX95022505FTE	13.5W	25M	100ppm
MOX96021005FVE	16W	10M	50ppm
MOX96025005FVE	16W	50M	50ppm
MOX96021006FVE	16W	100M	50ppm
MOX96021007FTE	16W	1000M	100ppm
MOX97021004FVE	20W	1M	50ppm
MOX97025004FVE	20W	5M	50ppm
MOX97021005FVE	20W	10M	50ppm
MOX97022505FTE	20W	25M	100ppm

Check product availability at **www.ohmite.com**

Series	Power Rating (W)	Max. Oper. Voltage	Res. Range (Ω)	Max. VCR*	Dimensions (In./mm) L	D
MOX910	3.80	15,000	1K-500M 500M-5G	0.40 0.75	1.07/27.00	0.32/8.00
MOX920	5.00	21,000	1K-1G 1G-10G	0.20 0.40	1.46/37.00	0.32/8.00
MOX930	7.50	30,000	1K-1G5 1G5-15G	0.15 0.30	2.05/52.00	0.32/8.00
MOX940	10.00	45,000	1K-2G5 2G5-25G	0.10 0.15	3.03/77.00	0.32/8.00
MOX950	13.50	60,000	1K-3G 3G-30G	0.08 0.12	4.02/102.00	0.33/8.30
MOX960	16.00	72,000	1K-4G 4G-40G	0.06 0.10	4.80/122.00	0.34/8.50
MOX970	20.00	90,000	1K-5G 5G-50G	0.04 0.08	5.98/152.00	0.34/8.50

* typical values, contact factory for details

ORDERING INFORMATION

Coating: conformal silicone standard; E = RoHS compliant

MOX910210006JTE

- **Super Mox Series** — see chart for wattage
- **Ohms** — First 3 digits are significant; 4th digit is multiplier (# of zeroes to follow). Examples: 10R2 = 10.2Ω; 1000 = 100Ω; 1503 = 150,000Ω; 1008 = 100 MΩ
- **Tolerance** — A = 0.05%, B = 0.10%, C = 0.25%, D = 0.5%, F = 1%, G = 2%, J = 5%, K = 10%
- **TCR** — T = 100ppm, V = 50ppm, W = 25ppm, X = 15ppm, Y = 10ppm

Our Tech Center is open 10am to 2pm CT Tuesdays and Thursdays, just call 866-9-OHMITE

Vishay Dale

Wirewound Resistors, Military, MIL-PRF-26 Qualified, Type RW, Precision Power, Silicone Coated

FEATURES

- High temperature coating (> 350 °C)
- Complete welded construction
- Meets applicable requirements of MIL-PRF-26
- Available in non-inductive styles (type NS) with Aryton-Perry winding for lowest reactive components
- Excellent stability in operation (typical resistance shift < 0.5 %)
- Lead (Pb)-Free version is RoHS Compliant

Pb-free Available

e3

RoHS* COMPLIANT

STANDARD ELECTRICAL SPECIFICATIONS

GLOBAL MODEL	HISTORICAL MODEL	MIL-PRF-26 TYPE	POWER RATING**** $P_{25\,°C}$ W U ± 0.05 % thru ± 5 %	POWER RATING**** $P_{25\,°C}$ W V ± 3 % thru ± 10 %	RESISTANCE RANGE MIL. RANGE SHOWN IN BOLD FACE Ω ± 0.05 %	± 0.1 %	± 0.25 %	± 0.5 % & ± 1 %	± 3 %, ± 5 %, ± 10 %	WEIGHT (Typical) g
RS1/8	RS-1B	—	0.125	—	—	—	—	0.1 - 950	0.1 - 950	0.15
RS1/4	RS-1/4	—	0.4	—	1 - 1 k	0.499 - 1k	0.499 - 3.4 k	0.1 - 3.4 k	0.1 - 3.4 k	0.21
RS1/2	RS-1/2	—	0.75	—	1 - 1.3 k	0.499 - 1.3k	0.499 - 4.9 k	0.1 - 4.9 k	0.1 - 4.9 k	0.23
RS01A	RS-1A	—	1.0	—	1 - 2.74 k	0.499 - 2.74 k	0.499 - 10.4 k	0.1 - 10.4 k	0.1 - 10.4 k	0.34
RS01A...300	RS-1A-300	RW70***	1.0 1.0	— —	—	0.499 - 2.74 k	0.499 - 10.4 k	0.1 - 10.4 k 0.1 - 2.74 k	0.1 - 10.4 k	0.34
RS01M	RS-1M	—	1.0	—	1 - 1.32 k	0.499 - 1.87 k	0.499 - 6.65 k	0.1 - 6.65 k	0.1 - 6.65 k	0.30
RS002	RS-2	—	4.0	5.5	0.499 - 12.7 k	0.499 - 12.7 k	0.1 - 47.1 k	0.1 - 47.1 k	0.1 - 47.1 k	2.10
RS02M	RS-2M	—	3.0	—	0.499 - 4.49 k	0.499 - 4.49 k	0.1 - 18.74 k	0.1 - 18.74 k	0.1 - 18.74 k	0.65
RS02B	RS-2B	—	3.0	3.75	0.499 - 6.5 k	0.499 - 6.5 k	0.1 - 24.5 k	0.1 - 24.5 k	0.1 - 24.5 k	0.70
RS02B...300	RS-2B-300	RW79***	3.0 3.0	— —	— —	0.499 - 6.5 k	0.1 - 24.5 k	0.1 - 24.5 k 0.1 - 6.49 k	0.1 - 24.5 k	0.70
RS02C	RS-2C	—	2.5	3.25	0.499 - 8.6 k	0.499 - 8.6 k	0.1 - 32.3 k	0.1 - 32.3 k	0.1 - 32.3 k	1.6
RS02C...17	RS-2C-17	—	2.5	3.25	0.499 - 6.8 k	0.499 - 8.6 k	0.1 - 32.3 k	0.1 - 32.3 k	0.1 - 32.3 k	1.6
RS02C...23	RS-2C-23	RW69**	—	3.25 3.0	—	—	—	—	0.1 - 32.3 k 0.1 - 2.0 k	16
RS005	RS-5	—	5.0	6.5	0.499 - 25.7 k	0.499 - 25.7 k	0.1 - 95.2 k	0.1 - 95.2 k	0.1 - 95.2 k	4.2
RS005...69	RS-5-69	RW74***	5.0 5.0	— —	—	0.499 - 25.7 k	0.1 - 95.2 k	0.1 - 95.2 k 0.1 - 24.3 k	0.1 - 95.2 k	4.2
RS005...70	RS-5-70	RW67***	— —	6.5 6.5	—	—	—	—	0.1 - 95.2 k 0.1 - 8.2 k	4.2
RS007	RS-7	—	7.0	9.0	0.499 - 41.4 k	0.499 - 41.4 k	0.1 - 154 k	0.1 - 154 k	0.1 - 154 k	4.7
RS010	RS-10	—	10.0	13.0	0.499 - 73.4 k	0.499 - 73.4 k	0.1 - 273 k	0.1 - 273 k	0.1 - 273 k	9.0
RS010...38	RS-10-38	RW78***	10.0 10.0	— —	—	0.499 - 73.4 k	0.1 - 273 k	0.1 - 273 k 0.1 - 71.5 k	0.1 - 273 k	9.0
RS010...39	RS-10-39	RW66**	— —	13.0 11.0	—	—	—	—	0.1 - 273 k 0.1 - 20 k	9.0

** Available tolerance for these Mil parts is ± 5 % for 1 Ω and above, ± 10 % below 1 Ω.
***Available tolerance for these Mil parts is ± 0.5 % & ± 1 % for resistance values 0.1 Ω and above, ± 0.1 % for resistance values 0.499 Ω and above.
****Vishay Dale RS models have two power ratings depending on operation temperature and stability requirements.
NOTE: Shaded area indicates most popular models.

GLOBAL PART NUMBER INFORMATION

New Global Part Numbering: RS02C10K00FS7017 (preferred part numbering format)

R	S	0	2	C	1	0	K	0	0	F	S	7	0	1	7	

GLOBAL MODEL	RESISTANCE VALUE	TOLERANCE CODE	PACKAGING	SPECIAL
(See Standard Electrical Specifications Global Model column for options)	R = Decimal K = Thousand 15R00 = 15 Ω 10K00 = 10 kΩ	A = ± 0.05 % B = ± 0.1 % C = ± 0.25 % D = ± 0.5 % F = ± 1.0 % J = ± 5.0 % K = 10.0 %	E70 = Lead (Pb)-free, Tape/Reel (smaller than RS005) E73 = Lead (Pb)-free, Tape/Reel (RS005 & larger) E12 = Lead (Pb)-free, Bulk Lead (Pb)-free is not available on RW military type S70 = Tin/Lead, Tape/Reel (smaller than RS005) S73 = Tin/Lead, Tape/Reel (RS005 & larger) B12 = Tin/Lead, Bulk	(Dash Number) (up to 3 digits) From 1-999 as applicable

Historical Part Number example: RS-2C-17 10 kΩ 1 % S70 (will continue to be accepted)

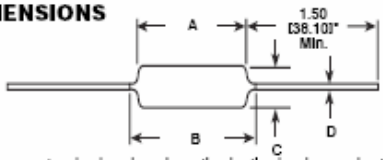
RS-2C-17	10 kΩ	1 %	S70
HISTORICAL MODEL	RESISTANCE VALUE	TOLERANCE CODE	PACKAGING

* Pb containing terminations are not RoHS compliant, exemptions may apply

For technical questions, contact ww2bresistors@vishay.com

Wirewound Resistors, Military, MIL-PRF-26 Qualified, Type RW, Precision Power, Silicone Coated

DIMENSIONS



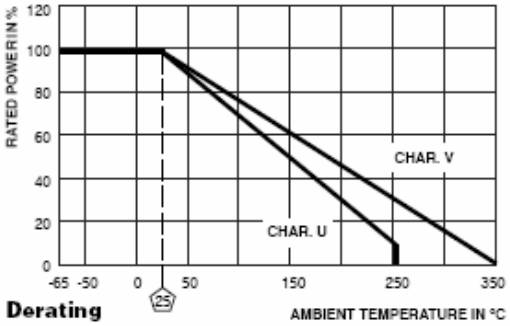
*On some standard reel pack methods, the leads may be trimmed to a shorter length than shown.
NOTE: RS-1/8 terminal length will be 1.0" [25.4 mm] minimum.

GLOBAL MODEL	DIMENSIONS in inches [millimeters]			
	A	B (Max.)**	C	D
RS1/8	0.155 ± 0.015 [3.94 ± 0.381]	—	0.065 ± 0.015 [1.65 ± 0.381]	0.020 ± 0.002 [0.508 ± 0.051]
RS1/4	0.250 ± 0.031 [6.35 ± 0.787]	0.281 [7.14]	0.085 ± 0.020 [2.16 ± 0.508]	0.020 ± 0.002 [0.508 ± 0.051]
RS1/2	0.312 ± 0.016 [7.92 ± 0.406]	0.328 [8.33]	0.078 + 0.016 - 0.031 [1.98 + 0.406 - 0.787]	0.020 ± 0.002 [0.508 ± 0.051]
RS01A RS01A...300	0.406 ± 0.031 [10.31 ± 0.787]	0.437 [11.10]	0.094 ± 0.031 [2.39 ± 0.787]	0.020 ± 0.002 [0.508 ± 0.051]
RS01M	0.285 ± 0.025 [7.24 ± 0.635]	0.311 [7.90]	0.110 ± 0.015 [2.79 ± 0.381]	0.020 ± 0.002 [0.508 ± 0.051]
RS002	0.625 ± 0.062 [15.88 ± 1.57]	0.765 [19.43]	0.250 ± 0.031 [6.35 ± 0.787]	0.040 ± 0.002 [1.02 ± 0.051]
RS02M	0.500 ± 0.062 [12.70 ± 1.57]	0.562 [14.27]	0.185 ± 0.015 [4.70 ± 0.381]	0.032 ± 0.002 [0.813 ± 0.051]
RS02B RS02B...300	0.560 ± 0.062 [14.22 ± 1.57]	0.622 [15.80]	0.187 ± 0.031 [4.75 ± 0.787]	0.032 ± 0.002 [0.813 ± 0.051]
RS02C	0.500 ± 0.062 [12.70 ± 1.57]	0.593 [15.06]	0.218 ± 0.031 [5.54 ± 0.787]	0.040 ± 0.002 [1.02 ± 0.051]
RS02C...17 RS02C...23	0.500 ± 0.062 [12.70 ± 1.57]	0.593 [15.06]	0.218 ± 0.031 [5.54 ± 0.787]	0.032 ± 0.002 [0.813 ± 0.051]
RS005 RS005...69 RS005...70	0.875 ± 0.062 [22.23 ± 1.57]	1.0 [25.4]	0.312 ± 0.031 [7.92 ± 0.787]	0.040 ± 0.002 [1.02 ± 0.051]
RS007	1.22 ± 0.062 [30.99 ± 1.57]	1.28 [32.51]	0.312 ± 0.031 [7.92 ± 7.87]	0.040 ± 0.002 [1.02 ± 0.051]
RS010 RS010...39	1.78 ± 0.062 [45.21 ± 1.57]	1.87 [47.50]	0.375 ± 0.031 [9.53 ± 0.787]	0.040 ± 0.002 [1.02 ± 0.051]
RS010...38	1.78 ± 0.062 [45.21 ± 1.57]	1.84 [46.74]	0.375 ± 0.031 [9.53 ± 0.787]	0.040 ± 0.002 [1.02 ± 0.051]

**B (Max.) dimension is clean lead to clean lead.

MATERIAL SPECIFICATIONS

Element: Copper-nickel alloy or nickel-chrome alloy, depending on resistance value
Core: Ceramic, steatite or alumina, depending on physical size
Coating: Special high temperature silicone
Standard Terminals: 100 % Sn, or 60/40 Sn/Pb coated Copperweld®.
NOTE: Military "RW" parts are only available with 60/40 Sn/Pb finish.
End Caps: Stainless steel
Deviations for RS-1/8: Thermoset silicone molded construction, endcaps will be nickel-silver alloy and terminals will be tinned copper
Part Marking: DALE, Model, Wattage*, Value, Tolerance, Date Code
*Wattage marked on part will be "U" characteristic



Derating

NS NON-INDUCTIVE

Models of equivalent physical and electrical specifications are available with non-inductive (Aryton-Perry) winding. They are identified by substituting the letter N for R in the model number (NS-5, for example).

Two conditions apply:
1. For NS models, divide maximum resistance values by two
2. Body O.D. on NS-2C may exceed that of the RS-2C by 010"

TECHNICAL SPECIFICATIONS

PARAMETER	UNIT	RS RESISTOR CHARACTERISTICS
Temperature Coefficient	ppm/°C	± 90 for below 1 Ω, ± 50 for 1 Ω to 9.9 Ω, ± 20 for 10 Ω and above
Dielectric Withstanding Voltage	V_{AC}	500 minimum for RS-1/8 thru RS-1A, 1000 minimum for all others
Maximum Working Voltage	V	$(P \times R)^{1/2}$
Insulation Resistance	Ω	1000 Megohm minimum dry, 100 Megohm minimum after moisture test
Terminal Strength	lb	5 minimum for RS-1/8 thru RS-1A, 10 minimum for all others
Solderability	–	MIL-PRF-26 type - Meets requirements of ANSI J-STD-002
Operating Temperature Range	°C	Characterisitic U = - 65/+ 250, Characteristic V = - 65/+ 350

PERFORMANCE*

TEST	CONDITIONS OF TEST	TEST LIMITS	
		Characteristic U	Characteristic V
Thermal Shock	Rated power applied until thermally stable, then a min. of 15 minutes at - 55 °C	± (0.2 % + 0.05 Ω) ΔR	± (2.0 % + 0.05 Ω) ΔR
Short Time Overload	5 x rated power (3.75 watt and smaller), 10 x rated power (4 watt and larger) for 5 seconds	± (0.2 % + 0.05 Ω) ΔR	± (2.0 % + 0.05 Ω) ΔR
Dielectric Withstanding Voltage	500 minimum for RS-1/8 thru RS-1A, 1000 for all others, duration of 1 minute	± (0.1 % + 0.05 Ω) ΔR	± (0.1 % + 0.05 Ω) ΔR
Low Temperature Storage	- 65 °C for 24 hours	± (0.2 % + 0.05 Ω) ΔR	± (2.0 % + 0.05 Ω) ΔR
High Temperature Exposure	250 hours at: U = + 250 °C, V = + 350 °C	± (0.5 % + 0.05 Ω) ΔR	± (2.0 % + 0.05 Ω) ΔR
Moisture Resistance	MIL-STD-202 Method 106, 7b not applicable	± (0.2 % + 0.05 Ω) ΔR	± (2.0 % + 0.05 Ω) ΔR
Shock, Specified Pulse	MIL-STD-202 Method 213, 100 g's for 6 milliseconds, 10 shocks	± (0.1 % + 0.05 Ω) ΔR	± (0.2 % + 0.05 Ω) ΔR
Vibration, High Frequency	Frequency varied 10 to 2000 Hz, 20 g peak, 2 directions 8 hours each	± (0.1 % + 0.05 Ω) ΔR	± (0.2 % + 0.05 Ω) ΔR
Load Life	2000 hours at rated power, + 25 °C, 1.5 hours "ON", 0.5 hours "OFF"	± (0.5 % + 0.05 Ω) ΔR	± (3.0 % + 0.05 Ω) ΔR
Terminal Strength	5 to 10 sec., 5 or 10 lb pull test (depending on size), torsion test - 3 alternating directions, 360° each	± (0.1 % + 0.05 Ω) ΔR	± (1.0 % + 0.05 Ω) ΔR

*All ΔR figures shown are maximum, based upon testing requirements per MIL-PRF-26.

The LM 411CN is the Operational Amplifier used in voltage divider and voltage probe circuit. These two pages are the first two pages only.

National Semiconductor

August 2000

LF411
Low Offset, Low Drift JFET Input Operational Amplifier

General Description

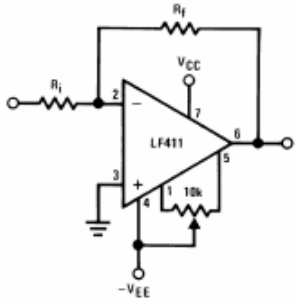
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage:	0.5 mV(max)
■ Input offset voltage drift:	10 µV/°C(max)
■ Low input bias current:	50 pA
■ Low input noise current:	0.01 pA/√Hz
■ Wide gain bandwidth:	3 MHz(min)
■ High slew rate:	10V/µs(min)
■ Low supply current:	1.8 mA
■ High input impedance:	$10^{12}\Omega$
■ Low total harmonic distortion:	≤0.02%
■ Low 1/f noise corner:	50 Hz
■ Fast settling time to 0.01%:	2 µs

Typical Connection



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Ordering Information

LF411XYZ

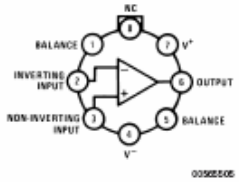
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



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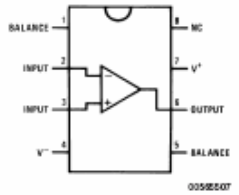
Note: Pin 4 connected to case.

Top View
Order Number LF411ACH
or LF411MH/883 (Note 11)
See NS Package Number H08A

Dual-In-Line Package



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Top View
Order Number LF411ACN, LF411CN
See NS Package Number N08E

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LF411 Low Offset, Low Drift JFET Input Operational Amplifier

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LF411A	LF411
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 2)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package
Power Dissipation (Notes 3, 10)	670 mW	670 mW

	H Package	N Package
$T_j$max	150°C	115°C
θ_jA	162°C/W (Still Air) 65°C/W (400 LF/min Air Flow)	120°C/W
θ_jC	20°C/W	
Operating Temp. Range	(Note 4)	(Note 4)
Storage Temp. Range	−65°C≤T_A≤150°C	−65°C≤T_A≤150°C
Lead Temp. (Soldering, 10 sec.)	260°C	260°C
ESD Tolerance	Rating to be determined.	

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF411A			LF411			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10 kΩ, T_A=25°C			0.3	0.5		0.8	2.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ (Note 6)			7	10		7	20 (Note 6)	µV/°C
I_{OS}	Input Offset Current	V_S=±15V (Notes 5, 7)	T_j=25°C		25	100		25	100	pA
			T_j=70°C			2			2	nA
			T_j=125°C			25			25	nA
I_B	Input Bias Current	V_S=±15V (Notes 5, 7)	T_j=25°C		50	200		50	200	pA
			T_j=70°C			4			4	nA
			T_j=125°C			50			50	nA
R_{IN}	Input Resistance	T_j=25°C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, V_O=±10V, R_L=2k, T_A=25°C		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	R_S≤10k		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	100		dB
I_S	Supply Current				1.8	2.8		1.8	3.4	mA

AC Electrical Characteristic (Note 5)

Symbol	Parameter	Conditions	LF411A			LF411			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	V_S=±15V, T_A=25°C	10	15		8	15		V/µs
GBW	Gain-Bandwidth Product	V_S=±15V, T_A=25°C	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω, f=1 kHz		25			25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_A=25°C, f=1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

The Arnold Powdered core is used to create the external leakage inductance to limit the change in current over change in time across the IGBTs of the VSI.

o.d. 2.250

i.d. 1.400/ht. 0.550

CORNERS:
0.094 Approx. Radius (Typical)

Dimensions

	Outside Diameter	Inside Diameter	Height
Before Coating Nominal	2.250 in 57.15 mm	1.400 in 35.56 mm	0.550 in 13.97 mm
After Coating (Blue Epoxy)	2.285 in Max. 58.04 mm Max.	1.368 in Min. 34.75 mm Min.	0.585 in Max. 14.86 mm Max.

Physical Specifications

Effective Cross Sectional Area of Magnetic Path, A_e (Reference)	Effective Magnetic Path Length, l_e (Reference)	Effective Core Volume, V_e (Reference)	Minimum Window Area (Reference)	Approximate Weight of Finished 125µ Core		Approximate Mean Length of Turn for Full Winding (Half of I.D. Remaining)
0.224 in² 1.444 cm²	5.628 in 14.296 cm	1.261 in³ 20.65 cm³	1.470 in² 9.483 cm² 1,871,424 cmil	MPP HF SMSS	170.000g 152.000g 126.000g	2.15 in 5.47 cm

Electrical Specifications

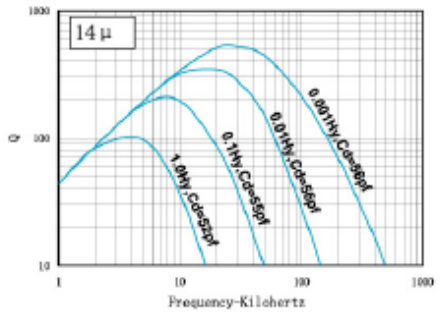
Nominal Permeability	Inductance Factor, mH +/- 8% for 1000 turns	Approximate Ratio of DC Resistance to Inductance for Full Winding (Half of I.D. Remaining), Ω/mH	Part Numbers			
			Molypermalloy		HI-FLUX	SUPER-MSS
			NEW	OLD		
14µ	18	0.12	MP-225014-2	A-096018-2	HF-225014-2	MS-225014-2
26µ	33	0.066	MP-225026-2	A-094033-2	HF-225026-2	MS-225026-2
60µ	75	0.029	MP-225060-2	A-488075-2	HF-225060-2	MS-225060-2
75µ	93.6	0.023	—	—	—	MS-225075-2
90µ	112	0.019	—	—	—	MS-225090-2
125µ	156	0.014	MP-225125-2	A-109156-2	HF-225125-2	MS-225125-2
147µ	185	0.012	MP-225147-2	A-155185-2	HF-225147-2	—
160µ	200	0.011	MP-225160-2	A-328200-2	HF-225160-2	—
173µ	218	0.010	MP-225173-2	A-182218-2	—	—
205µ	259	0.0084	MP-225205-2	A-218259-2	—	—

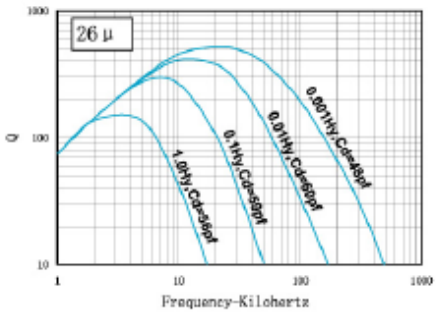
Heavy Film Magnet Wire Winding Data (Approximate)

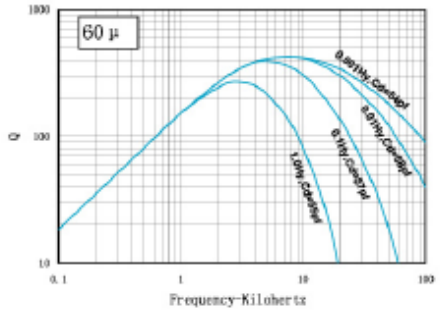
AWG	mm	Full Winding (Half of I.D. Remaining)		Single Layer Winding		
		Turns	R_{dc} Ω	Turns	R_{dc} Ω	l_w ft.
10	2.500	—	—	34	0.00649	6.50
11	2.240	—	—	38	0.00908	7.20
12	2.000	142	0.0435	43	0.0127	7.99
13	1.800	177	0.0677	48	0.0177	8.87
14	1.600	222	0.1057	54	0.0247	9.78
15	1.400	277	0.165	61	0.0346	10.9
16	1.250	347	0.258	68	0.0485	12.1
17	1.120	433	0.401	76	0.0678	13.4
18	1.000	541	0.628	86	0.0951	14.9
19	0.900	675	0.980	96	0.133	16.6
20	0.800	840	1.525	107	0.186	18.4
21	0.710	1046	2.38	120	0.261	20.5
22	0.630	1311	3.76	135	0.369	22.8
23	0.560	1622	5.80	150	0.512	25.2
24	0.500	2022	9.11	168	0.720	28.1
25	0.450	2514	14.22	188	1.01	31.3
26	0.400	3139	22.4	210	1.43	34.8
27	0.355	3880	34.6	233	1.98	38.6

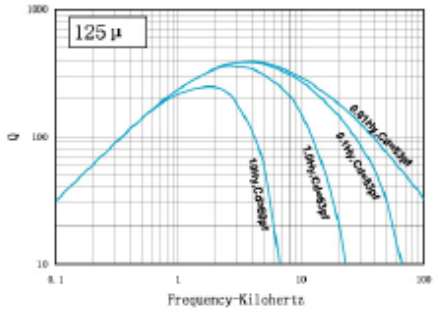
AWG	mm	Full Winding (Half of I.D. Remaining)		Single Layer Winding		
		Turns	R_{dc} Ω	Turns	R_{dc} Ω	l_w ft.
28	0.315	4850	54.8	260	2.80	42.9
29	0.280	5950	83.3	288	3.85	47.4
30	0.250	7473	133.3	322	5.48	52.9
31	0.224	9297	209.0	355	7.62	58.2
32	0.200	11380	316.0	392	10.4	64.1

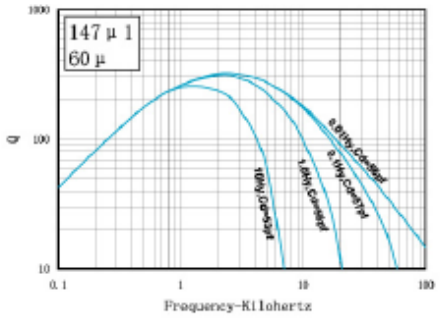
ARNOLD MAGNETIC TECHNOLOGIES

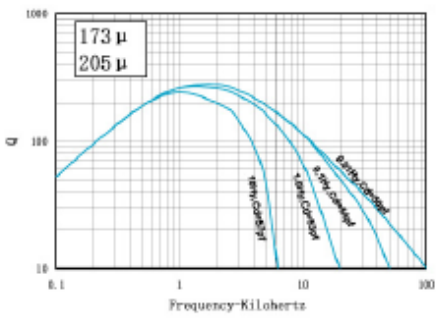












Typical Molypermalloy Q vs. frequency curves at indicated inductance and distributed capacitance.

The Metglas Powerlite C-core is the transformer core.

Metglas®

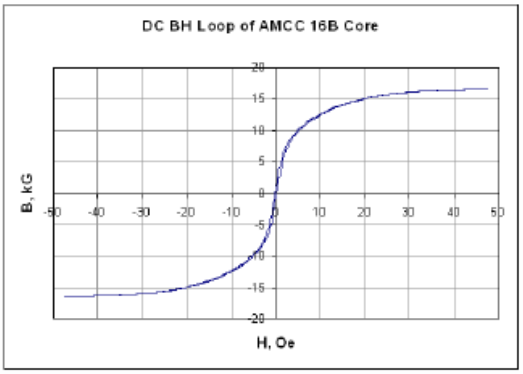
POWERLITE®
High Frequency Distributed Gap Inductor Cores

www.metglas.com

Technical Bulletin

POWERLITE® C-Cores are manufactured with iron based Metglas® amorphous Alloy 2605SA1. Their unique combination of low loss and high saturation flux density provide for size reduction and improvements in energy efficiency making them an ideal solution for automotive inductor applications

Typical DC Hysteresis Loop
Metglas® Alloy 2605SA1



Benefits

Manufactured in a variety of ultra-efficient core configurations, POWERLITE C-Cores provide significant cost, design and performance benefits over ordinary Si-Fe, ferrite and MPP cores such as:

- High Saturation Flux Density (1.56 T)
- Low Profile – enables weight and volume reductions of up to 50%
- Low Temperature Rise – enabling smaller compact designs
- Low Loss – resulting from micro-thin Metglas ribbon (25 µm)

Physical Properties METGLAS Alloy 2605SA1

Ribbon Thickness (µm)	.25
Density (g/cm3)	7.18
Thermal Expansion (ppm/°C)	7.6
Crystallization Temperature (°C)	505
Curie Temperature (°C)	392
Continuous Service Temperature (°C)	150
Tensile Strength (MN/m2)	1k-1.7k
Elastic Modulus (GN/m2)	100-110
Vicker's Hardness (50g load)	860

Magnetic Properties METGLAS Powerlite Cores

Saturation Flux Density (Tesla)	1.56
Permeability (depending on gap size)	VARIABLE
Saturation Magnetostriction (ppm)	27
Electrical Resistivity (µ Ω cm)	137

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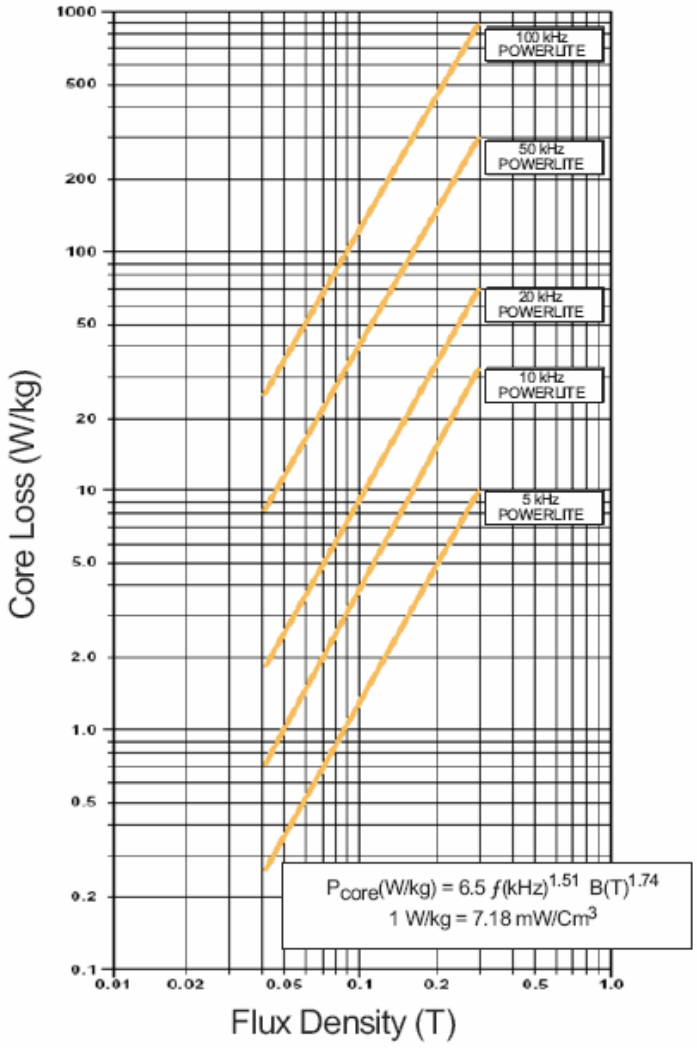
Core Loss vs. Flux Density* @ 25°C



* *These curves were determined from ac data; use 1/2 the actual .B to determine core loss for unidirectional applications.*

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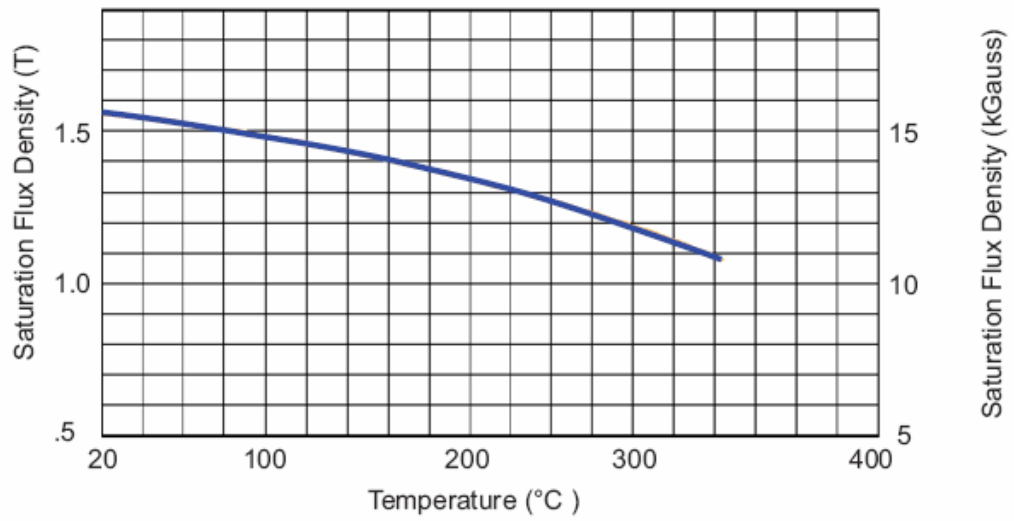
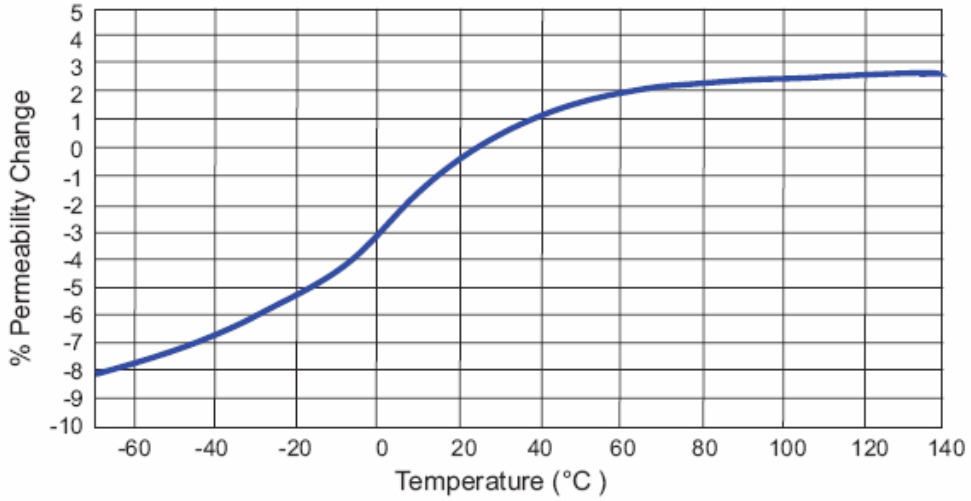
Saturation Induction vs. Temperature



Permeability vs. Temperature



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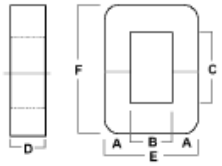
Standard Core Specifications

AMCC1000

Amorphous Metal

C-Core

Part Designation



	Core Dimensions										Performance Parameters				
	a(mm)	±	b(mm) ref	c(mm) ref	d(mm)	±	e(mm)	±	f(mm)	±	(lm) cm	ac (cm^2)	Wa (cm^2)	Ap (cm^4)	(gms)
AMCC 4	9.00	0.50	10.50	32.75	15.25	0.25	28.50	0.50	51.00	1.00	12.70	1.11	3.44	3.82	102
AMCC 6.3	10.0	0.50	11.00	33.0	20.00	0.50	31.00	1.00	53.00	2.00	13.10	1.60	3.60	5.80	150
AMCC 10	11.0	0.80	13.00	40.0	20.00	0.50	35.00	1.00	62.00	2.00	15.40	1.80	5.20	9.40	200
AMCC 8	11.0	0.80	13.00	30.0	20.00	0.50	35.00	1.00	52.00	2.00	13.20	1.80	3.90	7.00	170
AMCC 16B	11.0	0.80	13.00	50.0	25.00	0.50	35.00	1.00	72.00	2.00	16.90	2.30	6.50	15.0	280
AMCC 16A	11.0	0.80	13.00	40.0	25.00	0.50	35.00	1.00	62.00	2.00	15.10	2.30	5.20	12.0	250
AMCC 20	11.0	0.80	13.00	50.0	30.00	0.50	35.00	1.00	72.00	2.00	17.50	2.70	6.50	17.6	340
AMCC 40	13.0	0.80	15.00	56.0	35.00	0.50	41.00	1.00	82.00	2.00	19.90	3.70	8.40	31.1	530
AMCC 25	13.0	0.80	15.00	56.0	25.00	0.50	41.00	1.00	82.00	2.00	19.60	2.70	8.40	22.7	380
AMCC 32	13.0	0.80	15.00	56.0	30.00	0.50	41.00	1.00	82.00	2.00	20.00	3.20	8.40	26.9	460
AMCC 50	16.0	1.00	20.00	70.0	25.00	0.50	52.00	1.00	102.0	3.00	24.90	3.30	14.0	46.2	590
AMCC 63	16.0	1.00	20.00	70.0	30.00	0.50	52.00	1.00	102.0	3.00	25.30	3.90	14.0	54.6	710
AMCC 80	16.0	1.00	20.00	70.0	40.00	1.00	52.00	1.00	102.0	3.00	25.40	5.20	14.0	72.8	950
AMCC 100	16.0	1.00	20.00	70.0	45.00	1.00	52.00	1.00	102.0	3.00	25.00	5.90	14.0	82.6	1,060
AMCC 160	19.0	1.00	25.00	83.0	40.00	1.00	63.00	1.00	121.0	3.00	28.50	6.50	20.8	135.2	1,330
AMCC 125	19.0	1.00	25.00	83.0	35.00	1.00	63.00	1.00	121.0	3.00	30.20	5.40	20.8	112.1	1,170
AMCC 250	19.0	1.00	25.00	90.0	60.00	1.00	63.00	1.00	128.0	3.00	31.40	9.30	22.5	209.3	2,100
AMCC 200	19.0	1.00	25.00	83.0	50.00	1.00	63.00	1.00	121.0	3.00	29.80	7.80	20.8	162.2	1,670
AMCC 168S	20.4	0.50	30.20	155.2	20.00	0.50	71.00	0.75	196.0	2.00	45.40	3.35	45.7	153.0	1,090
AMCC 320	22.0	1.00	35.00	85.0	50.00	1.00	79.00	1.00	129.0	4.00	32.50	9.00	29.8	267.8	2,170
AMCC 400	22.0	1.00	35.00	85.0	65.00	1.00	79.00	1.00	129.0	4.00	33.60	11.7	29.8	348.1	2,820
AMCC 500	25.0	1.00	40.00	85.0	55.00	1.00	90.00	1.00	135.0	4.00	35.60	11.3	34.0	384.2	2,900
AMCC 630	25.0	1.00	40.00	85.0	70.00	1.00	90.00	1.00	135.0	4.00	35.60	14.3	34.0	486.2	3,670
AMCC 800A	25.0	1.00	40.00	85.0	85.00	1.50	90.00	1.00	135.0	4.00	35.60	17.4	34.0	591.6	4,450
AMCC 367S	25.8	1.00	66.00	97.8	25.00	0.70	117.6	1.50	149.4	1.50	43.78	5.29	63.8	338.0	1,662
AMCC 800B	30.0	1.00	40.00	95.0	85.00	1.50	100.0	1.00	155.0	4.00	39.30	21.0	38.0	798.0	5,930
AMCC 1000	33.0	1.00	40.00	105.0	85.00	1.50	106.0	1.00	171.0	5.00	42.70	23.0	42.0	966.0	7,060

The manufacturer ensures that the outer dimensions and weight of each individual core conforms to specifications. However, core profile and inner window dimensions are shown for reference and only minimum dimensions are ensured.

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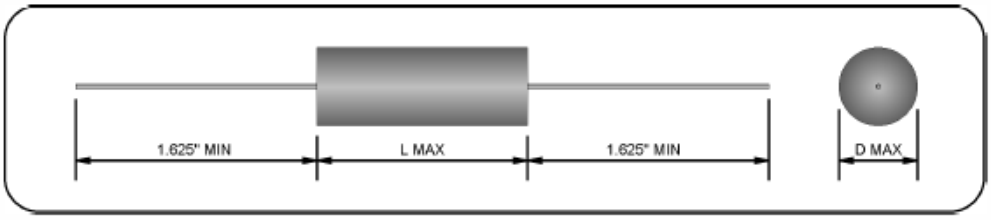
These ASC capacitors are used in the high voltage rectifier doubler.

ASC CAPACITORS

METALLIZED POLYESTER TAPE WRAP AND EPOXY FILL CASE **X675**



6000VDC				
CAP (µF)	D MAX	L MAX	LEAD AWG	I_{PEAK} (A)
0.0010	0.320" (8.1mm)	1.664" (42.3mm)	22	0.2
0.0015	0.330" (8.4mm)	1.664" (42.3mm)	22	0.3
0.0022	0.350" (8.9mm)	1.664" (42.3mm)	22	0.4
0.0033	0.400" (10.2mm)	1.664" (42.3mm)	22	0.6
0.0047	0.430" (10.9mm)	1.664" (42.3mm)	20	0.8
0.0068	0.500" (12.7mm)	1.664" (42.3mm)	20	1.2
0.010	0.580" (14.7mm)	1.664" (42.3mm)	20	1.7
0.015	0.680" (17.3mm)	1.664" (42.3mm)	20	2.6
0.022	0.800" (20.3mm)	1.664" (42.3mm)	20	3.8
0.033	0.650" (16.5mm)	2.664" (67.7mm)	20	3.4
0.047	0.740" (18.8mm)	2.664" (67.7mm)	20	4.8
0.068	0.880" (22.4mm)	2.664" (67.7mm)	20	6.9
0.10	1.060" (26.9mm)	2.664" (67.7mm)	20	10.2
0.15	1.200" (30.5mm)	2.664" (67.7mm)	20	15.3

8000VDC				
CAP (µF)	D MAX	L MAX	LEAD AWG	I_{PEAK} (A)
0.0010	0.320" (8.1mm)	2.034" (51.7mm)	22	0.2
0.0015	0.350" (8.9mm)	2.034" (51.7mm)	22	0.3
0.0022	0.380" (9.7mm)	2.034" (51.7mm)	22	0.5
0.0033	0.430" (10.9mm)	2.034" (51.7mm)	20	0.7
0.0047	0.480" (12.2mm)	2.034" (51.7mm)	20	1.1
0.0068	0.560" (14.2mm)	2.034" (51.7mm)	20	1.5
0.010	0.660" (16.8mm)	2.034" (51.7mm)	20	2.3
0.015	0.780" (19.8mm)	2.034" (51.7mm)	20	3.4
0.022	0.940" (23.9mm)	2.034" (51.7mm)	20	5.0
0.033	1.110" (28.2mm)	2.034" (51.7mm)	20	7.5
0.047	0.830" (21.1mm)	3.344" (84.9mm)	20	6.2
0.068	1.025" (26.0mm)	3.344" (84.9mm)	20	9.0
0.10	1.250" (31.8mm)	3.344" (84.9mm)	20	13.2

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Fax: (308) 284-8324
e-mail: sales@ascapacitor.com
web: www.ascapacitor.com

GENERAL SPECIFICATIONS

PHYSICAL CHARACTERISTICS

CONSTRUCTION: NON-INDUCTIVE WOUND METALLIZED POLYESTER.

CASE: FLAME RETARDANT TAPE WRAP CASE AND EPOXY FILL.

LEAD MATERIAL: AXIAL SOLDER COATED OR TINNED SOLID WIRE, AWG AS SPECIFIED IN TABLES.

DIMENSIONS: AS SPECIFIED IN TABLES.

ELECTRICAL CHARACTERISTICS

CAPACITANCE: AS SPECIFIED IN TABLES ± REQUESTED TOLERANCE WHEN MEASURED AT OR REFERRED TO 1000 ± 20 Hz AND 25 ± 5 °C.

TOLERANCE: ±5%, ±10%, AND ±20% AVAILABLE. OTHER TOLERANCES AVAILABLE UPON REQUEST.

DISSIPATION FACTOR: SHALL NOT BE GREATER THAN 1.0% WHEN MEASURED AT OR REFERRED TO 1000 ± 20 Hz AND 25 ± 5 °C.

INSULATION RESISTANCE: SHALL BE GREATER THAN 25,000 MΩ FOR CAPACITANCE VALUES 0.40 µF AND LESS OR 10,000 MΩ X µF FOR CAPACITANCE VALUES GREATER THAN 0.40 µF WHEN MEASURED AFTER 2 MINUTES ELECTRIFICATION AT 500VDC AND 25 ± 5 °C.

DIELECTRIC STRENGTH: 140% RATED VOLTAGE FOR 10 SECONDS THROUGH A LIMITING RESISTANCE OF 100 OHMS/VOLT AT 25 ± 5 °C.

RATED VOLTAGE: 2000VDC, 4000VDC, 6000VDC, 8000VDC, 10000VDC, AND 16000VDC AVAILABLE.

TEMPERATURE: -55 °C TO +85 °C AT FULL RATED VOLTAGE OPERATIONAL TEMPERATURE, TO +85 °C WITH 25% VOLTAGE DERATING, +105 °C MAX STORAGE TEMPERATURE.

ADDITIONAL INFORMATION

ORDERING INFORMATION: ALL ASC CAPACITORS ARE ORDERED BY "FAMILY CAP-TOL-VOLT" DESIGNATION. (I.E. TO ORDER AN X675 0.047µF, ±5%, 10000VDC CAPACITOR, REQUEST PART NUMBER "X675 .047-5-10000")

SEE ALSO: "GENERAL INFORMATION - POLYESTER CAPACITORS" DOCUMENT FOR ADDITIONAL PHYSICAL, ELECTRICAL, AND PERFORMANCE CHARACTERISTICS NOT MENTIONED IN THIS FILE.

WARNING: INFORMATION ON THIS FILE IS SUBJECT TO CHANGE WITHOUT NOTICE AT ASC'S DISCRETION.

LAST MODIFIED: 08/23/01

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e-mail: sales@ascapacitor.com
web: www.ascapacitor.com

These Vishay diodes are used on the high voltage doubler rectifier.

VISHAY

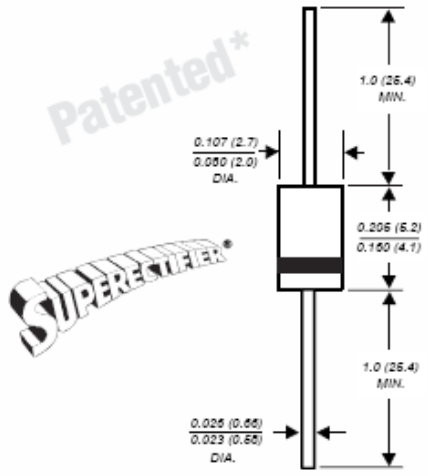
RGP02-12E THRU RGP02-20E

Vishay Semiconductors
formerly General Semiconductor

Case Style GP10E

Glass Passivated Junction Fast Switching Rectifier

Reverse Voltage 1200 to 2000V
Forward Current 0.5A



Dimensions in inches and (millimeters)
**Glass-plastic encapsulation technique is covered by Patent No. 3,996,602, and brazed-lead assembly by Patent No. 3,030,306*

Features

- Plastic package has Underwriters Laboratories Flammability Classification 94V-0
- High temperature metallurgically bonded construction
- Capable of meeting environmental standards of MIL-S-19500
- For use in high frequency rectifier circuits
- Fast switching for high efficiency
- Cavity-free glass passivated junction
- 0.5 Ampere operation at T_A=55°C with no thermal runaway
- Typical I_R less than 0.2µA
- High temperature soldering guaranteed: 350°C/10 seconds, 0.375" (9.5mm) lead length, 5 lbs. (2.3kg) tension

Mechanical Data

Case: Molded plastic over glass body
Terminals: Plated axial leads, solderable per MIL-STD-750, Method 2026
Polarity: Color band denotes cathode end
Mounting Position: Any
Weight: 0.012 oz., 0.3 g

Maximum Ratings & Thermal Characteristics

Ratings at 25°C ambient temperature unless otherwise specified.

Parameter	Symbols	RGP02 -12E	RGP02 -14E	RGP02 -16E	RGP02 -18E	RGP02 -20E	Units
Maximum repetitive peak reverse voltage	V_{RRM}	1200	1400	1600	1800	2000	V
Maximum RMS voltage	V_{RMS}	840	980	1120	1260	1400	V
Maximum DC blocking voltage	V_{DC}	1200	1400	1600	1800	2000	V
Maximum average forward rectified current 0.375" (9.5mm) lead length at T_A=55°C	$I_{F(AV)}$	0.5					A
Peak forward surge current 8.3ms single half sine-wave superimposed on rated load (JEDEC Method)	I_{FSM}	20					A
Typical thermal resistance (1)	$R_{\theta JA}$ $R_{\theta JL}$	65 30					°C/W
Operating junction and storage temperature range	T_J, T_{STG}	-65 to +175					°C

Electrical Characteristics

Ratings at 25°C ambient temperature unless otherwise specified.

Maximum instantaneous forward voltage at 0.1A	V_F	1.8	V
Maximum DC reverse current at rated DC blocking voltage T_A=25°C T_A=125°C	I_R	5.0 50	µA
Maximum reverse recovery time at I_F=0.5A, I_R=1.0A, I_{rr}=0.25A	t_{rr}	300	ns
Typical junction capacitance at 4.0V, 1MHz	C_J	5.0	pF

Note:
(1) Thermal resistance from junction to ambient and from junction to lead at 0.375" (9.5mm) lead length, P.C.B. mounted

Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 1 — Forward Current Derating Curve

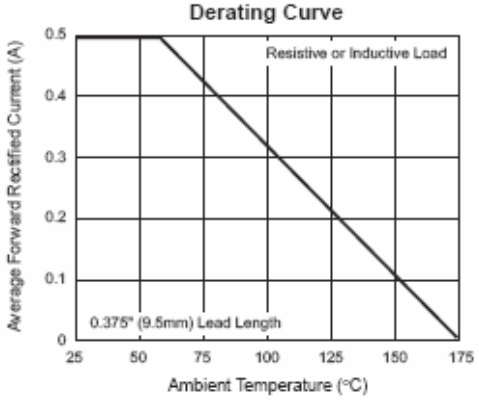


Fig. 2 — Maximum Non-Repetitive Peak Forward Surge Current

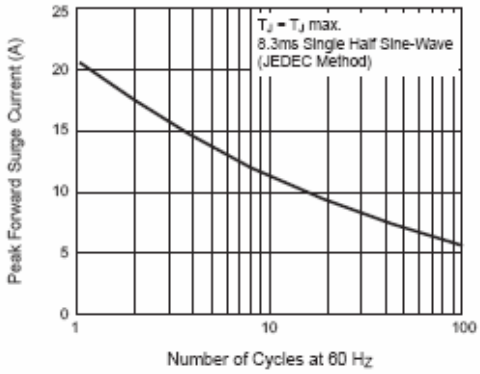


Fig. 3 — Typical Instantaneous Forward Characteristics

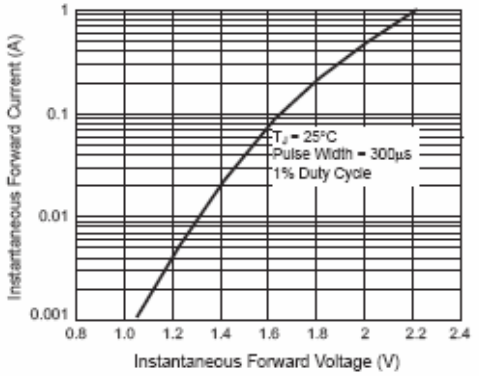


Fig. 4 — Typical Reverse Characteristics

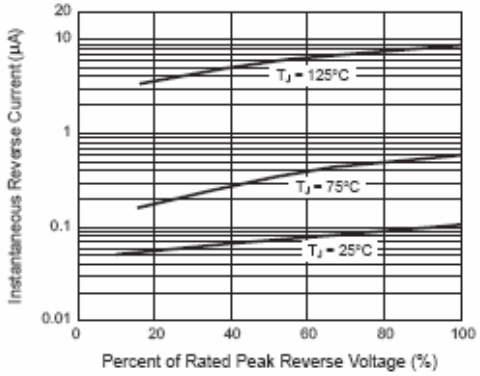
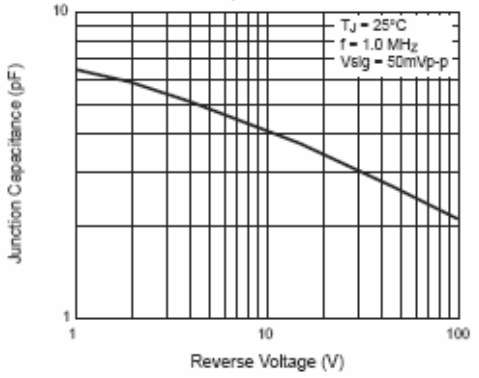


Fig. 5 — Typical Junction Capacitance



This information is for the Ohmite resistors; the 10Ω and the 100Ω in the high voltage doubler rectifier circuit.

Technical/Catalog Information	**AW101KE**
Vendor	Ohmite
Category	Resistors
Mounting Type	Through Hole
Package Name	Radial
Resistance	100.00 Ohms [Typ]
Resistance Tolerance	±10%
Power	2.50 W [Max]
Working Voltage	1500.000 V [Max]
Diameter	13.0000 mm [Typ]
Length	20.000 mm [Typ]
Packaging	Bulk
Energy	400.000 J [Max]
T081 Catalog Page	1696 [Nom]
Height	22.000 mm [Typ]
D	13.000 mm [Typ]
H	22.000 mm [Typ]
L	20.000 mm [Typ]
S	17.500 mm [Typ]
Lead Free Status	Lead Free
RoHS Status	RoHS Compliant
Other Names	AW101KE AW101KE

Technical/Catalog Information	**AW100KE**
Vendor	Ohmite
Category	Resistors
Mounting Type	Through Hole
Package Name	Radial
Resistance	10.00 Ohms [Typ]
Resistance Tolerance	±10%
Power	2.50 W [Max]
Working Voltage	1500.000 V [Max]
Diameter	13.0000 mm [Typ]
Length	20.000 mm [Typ]
Packaging	Bulk
Energy	400.000 J [Max]
T081 Catalog Page	0 [Nom]
Height	22.000 mm [Typ]
D	13.000 mm [Typ]
H	22.000 mm [Typ]
L	20.000 mm [Typ]
S	17.500 mm [Typ]
Lead Free Status	Lead Free
RoHS Status	RoHS Compliant
Other Names	AW100KE AW100KE

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